M21235-34

Wideband (HD/SD-SDI) Auto-rate Reclocker w/4:1 Selector

Rev V1

Applications

- Serial Routing Switchers
- Distribution Amplifiers
- SMPTE Coaxial Cable Interface
- Studio video applications
- Broadcast video applications
- Distribution video applications

Standards Compliance

- SMPTE 259M, 292M, 344M and DVB-ASI

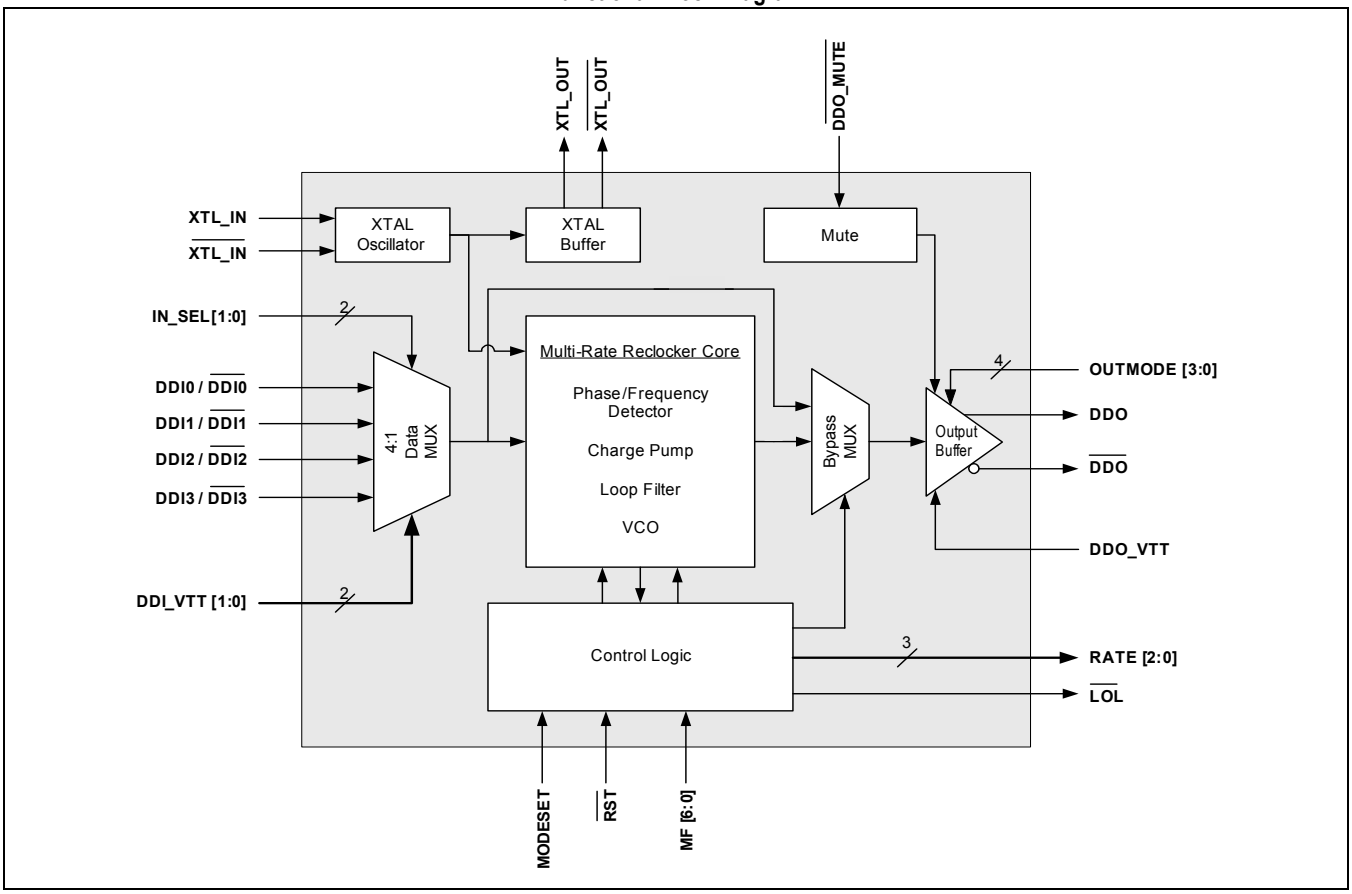
Features

- Data rate support for 143, 177, 270, 360, 540, 1483.5, 1485 Mbps and DVB-ASI at 270 Mbps
- Auto and manual rate selection modes with rate indication in Auto
- 4:1 Input MUX and Loss of Lock (LOL) indicator
- Differential I/O with on chip termination resistors
- Selectable auto MUTE or BYPASS with manual BYPASS option
- Low typical power dissipation (400 mW @ 3.3V)
- 2.5V, or 3.3V power supply operation
- Extended temperature operation: -10°C to +85°C
- 7 x 7 mm, 48-pin MLF package

The M21235 is a high-speed, low-power reclocker designed to remove both random and inter-symbol interference (ISI) jitter from the retimed data for SMPTE (292M, 259M, 344M) and DVB-ASI serial digital video applications.

The M21235 design is based on a robust and proven reclocker architecture widely deployed in telecom and data-com systems. A custom and proprietary phase detector which combines the best of linear and non-linear phase detectors is used for high-jitter tolerance, especially, in the presence of duty-cycle-distortion (DCD) that typically arises with AC coupling and video pathological test patterns. The M21235 offers a variety of features that are accessible through multifunctional (MF) hardware pins or through a two-wire, I^2C-compatible serial programming interface.

Functional Block Diagram



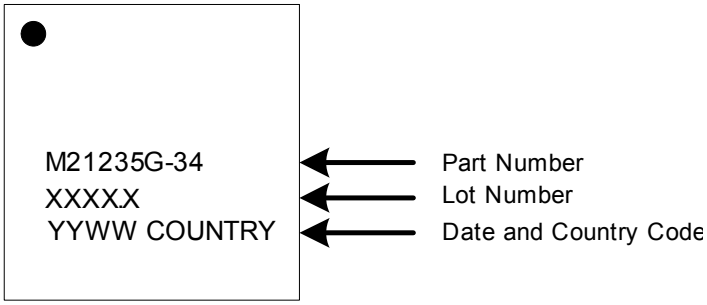
Ordering Information

Part Number	Package	Operating Temperature
M21235G-34*	48-pin, 7 mm x 7 mm MLF, (RoHS compliant)	–10 °C to 85 °C
*The G in the part number indicates that this is an RoHS compliant package.		

Revision History

Revision	Level	Date	Description
V1	Release	December 2015	Updated package drawing, Figure 1-1. Package effective as of August 2014. Added Figure 1-2. Added marking diagram. Removed preliminary markers.
V2P	Preliminary	May 2015	Updated logos and page layout. No content changes.
C (V1P)	Preliminary	May 2006	Preliminary Release
B (V2A)	Advance	May 2005	General update. -33P added.
A (V1A)	Advance	November 2004	Initial Release

M21235 Marking Diagram



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1.0 Product Specifications

1.1 General Specifications

Table 1-1. Absolute Maximum Ratings

Symbol	Item	Minimum	Maximum	Units
DV_{DD}	Digital I/O Power	V_{SS}-0.5	V_{SS} + 3.6	V
AV_{DD}	Analog I/O Power	V_{SS}-0.5	V_{SS} + 3.6	V
T_{STORE}	Storage Temperature	–65	+150	°C
ESD_{HBML}	Human Body Model (low-speed)	2000	—	V
ESD_{HBMH}	Human Body Model (high-speed)	2000	—	V
ESD_{CDM}	Charge Device Model	500	—	V
I_{DC}	Maximum DC Input Current	—	25	mA

NOTE:

1. No Damage

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
AV_{DD}	AV_{DD}: Analog Power	—	2.375	2.5/3.3	3.47	V
DV_{DD}	DV_{DD}: Digital Power	—	2.375	2.5/3.3	3.47	V
V_{SS}	V_{SS}: Chip Ground	—	—	0	—	V
T_{AMB}	Ambient Temperature	1	-10	—	+85	°C
θ_{JA}	Junction to ambient Thermal Resistance	1	—	29.4	—	°C/W

NOTES:

1. Soldered on multilayer board (≥ 4 layers), airflow = 0.0 m/s.

Table 1-3. Power DC Electrical Specifications

Symbol	Item	Notes	Minimum	Typical	Maximum	Units
Total I_{DD}	Total I_{DD}(constant for all supply voltages)	1, 3	—	122	140	mA
Total P_{DISS}	Total P_{DISS} (@2.5V)	1, 2, 3	—	325	370	mW
Total P_{DISS}	Total P_{DISS} (@3.3V)	1, 2, 3	—	430	485	mW

NOTES:

1. Recommended operating conditions - see Table 1-2.
2. Typical calculated at nominal supply voltage, maximum calculated at nominal supply voltage +5%.
3. Measured in hardware mode, output swing = 800 mV.

1.2 Input/Output Level Specifications:

Table 1-4. CMOS I/O Electrical Specifications

Symbol	Item	Notes	Minimum	Typical	Maximum	Units
V_{OH}	Output Logic High	1	0.8 x DV_{DD}	DV_{DD}	—	V
V_{OL}	Output Logic Low	1	—	0.0	0.2 x V_{DD}	V
I_{OH}	Output Current (logic high)	1	-10	—	0	mA
I_{OL}	Output Current (logic low)	1	0	—	10	mA
V_{IH}	Input Logic High	1	0.75 x V_{DD}	—	3.6	V
V_{IL}	Input Logic Low	1	0	—	0.25 x V_{DD}	V
I_{IH}	Input Current (logic high)	1	-100	—	100	µA
I_{IL}	Input Current (logic low)	1	-100	—	100	µA
t_r	Output Rise Time (20-80%)	1	—	—	10	ns
t_f	Output Fall Time (20-80%)	1	—	—	10	ns

NOTE:

1. Specified at recommended operating conditions - see Table 1-2. Specification is for a maximum load of 20 pF

Table 1-5. High-Speed Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input Bit Rate (reclocker bypassed)	1	0	—	1500	Mbps
	Input Bit Rate (reclocker enabled)	1	143	—	1485	Mbps
V_{ID}	Input Differential Voltage (peak - peak)	1, 2, 3	100	—	2000	mV
V_{ICM}	Input Common-Mode Voltage	1	V_{SS} + 1.15	—	AV_{DD}	V
V_{IMAX}	Maximum Input High Voltage	1	—	—	AV_{DD} + 400	mV
V_{IMIN}	Minimum Input Low Voltage	1	V_{SS}+1.0	—	—	V
ΔV_{TT}	Max Common-Mode Voltage to **DDI_VTT[1:0]** Voltage difference	1	—	—	600	mV
R_{IN}	**DDI_VTT[1:0]** input termination impedance to AV_{DD}	1	40	50	60	Ω

NOTES:

1. Specified at recommended operation conditions - see Table 1-2
2. Example 1200 mV_{pp} differential = 600 mV_{pp} for each single-ended terminal
3. Min. input level defined as error free operation at 10^{-12} BER with PRBS input pattern

Table 1-6. Output Electrical Specifications

Parameter		Symbol	Notes	Minimum	Typical	Maximum	Units
OUTMODE[1:0]	OUTMODE[3:2]						
OUTMODE[1:0] = 00b CML Output Mode	Common Mode Voltage POWERDOWN = 00b	V_{OCM}	1, 2		floating		
	Differential Output Voltage POWERDOWN = 00b	V_{OD}	1, 2		0		V
	Common Mode Voltage Low Swing PCML = 01b	V_{OCM}	1, 2		AV_{DD} - 0.175		V
	Differential Output Voltage Low Swing PCML = 01b	V_{OD}	1, 2	300	450	600	mV_{PP}
	Common Mode Voltage Medium Swing PCML = 10b	V_{OCM}	1, 2		AV_{DD} - 0.25		V
	Differential Output Voltage Medium Swing PCML = 10b	V_{OD}	1, 2	600	800	1000	mV_{PP}
	Common Mode Voltage High Swing PCML = 11b [Default Setting]	V_{OCM}	1, 2		AV_{DD} - 0.5		V
	Differential Output Voltage High Swing PCML = 11b [Default Setting]	V_{OD}	1, 2, 3	1300	1600	2000	mV_{PP}
V_{DDO_TERM}	Termination impedance to V_{DD}	R_O	1	40	50	60	Ω

NOTES:

1. Specified at recommended operating conditions – see Table 1-2
2. With 50Ω to AV_{DD} termination.
3. Only valid with AV_{DD} = 3.3V

Table 1-7. Reference Clock Input

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
F_{REF}	Input reference source or crystal rate	1, 2	—	12.000/14.140	—	MHz
V_{REFIN}	Input Differential Voltage Swing (peak-peak)	1, 3	100	200	1600	mV
V_{ICM}	Input Common-Mode Voltage	1, 3	250	—	AV_{DD} -1200	mV
I_{DC}	Maximum DC input current	1	—	—	15	mA

NOTES:

1. Specified at recommended operation conditions - see Table 1-2
2. The default value is 14.140 MHz crystal; however, a 12.00 MHz crystal can also be used (see text for more information)
3. Designed to accept a crystal, CMOS oscillator, or CMOS system clock. CMOS oscillator or system clock can be single-ended or differential

1.3 Reclocker Performance Specifications

Table 1-8. Reclocker Output Jitter Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
J_{ERMS}	Reclocker Enabled Output Data Jitter @ 1.485 Gbps (RMS)	1, 2, 3	—	5.5	9	ps
J_{EP-P}	Reclocker Enabled Output Data Jitter @ 1.485 Mbps (pp)	1, 2, 3	—	56	80	mUI
J_{EP-P}	Reclocker Enabled Output Data Jitter @ < 600 Mbps (pp)	1, 2, 3	—	—	40	mUI
J_{BRMS}	Reclocker Bypassed Output Data Jitter @ 1.485 Gbps (RMS)	1, 2, 3	—	5	—	ps
J_{BP-P}	Reclocker Bypassed Output Data Jitter @ 1.485 Gbps (pp)	1, 2, 3	—	—	52	mUI
J_{BP-P}	Reclocker Bypassed Output Data Jitter @ < 600 Mbps (pp)	1, 2, 3	—	—	30	mUI

NOTES:

1. Specified at recommended operation conditions - see Table 1-2
2. All jitter is measured using a 2^{23}-1 PRBS pattern, and/or HD/SD-SDI color bar test pattern.
3. All jitter is measured using a wideband scope (minimum 10 GHz bandwidth).

Table 1-9. Reclocker High-speed Performance

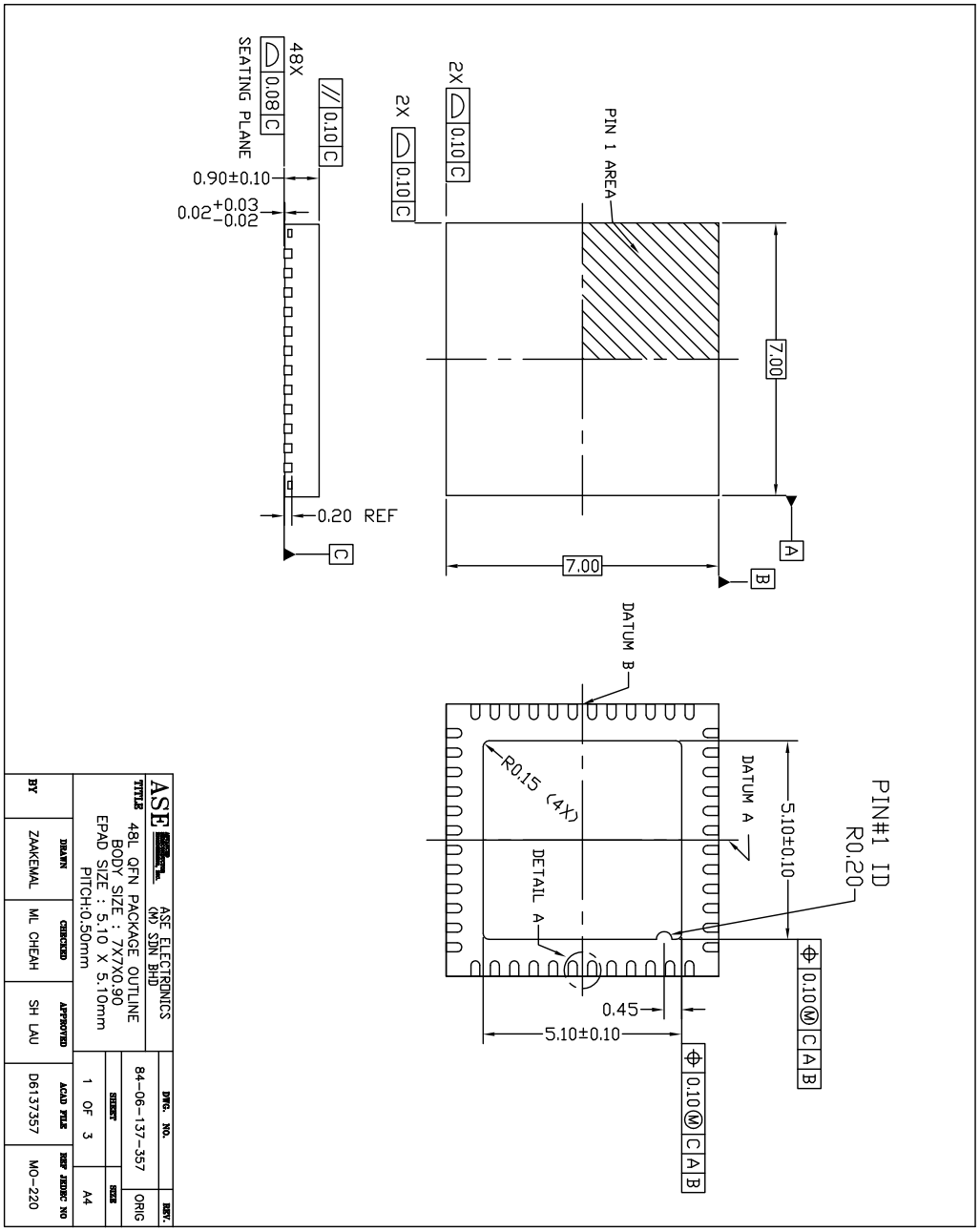
Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input Bit Rate (NRZ data - Reclocker enabled)	1, 2	143	—	1485	Mbps
J_{TOL}	Input jitter tolerance (10 Hz to 0.5 x LBW)	1, 3	1.2	—	—	UI
J_{TOL}	Input jitter tolerance (1.5xLBW to 10 MHz)	1, 3	0.6	—	—	UI
J_{GRMS}	Jitter Generation (rms) @ 1.485 Gbps	1, 3	—	6	—	mUI
J_{GP-P}	Jitter Generation (pp) @ 1.485 Gbps	1, 3	—	36	—	mUI
LBW_{HD}	Loop bandwidth **LBW_INC[1:0]** = 11b at 1.485 Gbps	1	—	—	1.5	MHz
LBW_{HD}	Loop bandwidth **LBW_INC[1:0]** = 10b at 1.485 Gbps	1	—	—	3.5	MHz
LBW_{HD}	Loop bandwidth **LBW_INC[1:0]** = 00b at 1.485 Mbps	1	—	—	5	MHz
LBW_{SD}	Loop bandwidth **LBW_INC[1:0]** = 11b at 270 Mbps	1	—	—	0.520	MHz
LBW_{SD}	Loop bandwidth **LBW_INC[1:0]** = 10b at 270 Mbps	1	—	—	1	MHz
LBW_{SD}	Loop bandwidth **LBW_INC[1:0]** = 00b at 270 Mbps	1	—	—	1.4	MHz
LBW_{PK}	Loop bandwidth peaking (270 - 1485 Mbps)	1	—	0.1	—	dB
t_{LKA}	Asynchronous Lock (Auto Rate Detect lock time)	1, 4	—	2	3	ms
t_{LKS}	Synchronous Switch Lock TIme @ 1.485 Gbps	1, 4	—	110	150	ns
t_{LKS}	Synchronous Switch Lock TIme @ 270 Mbps	1, 4	—	330	400	ns

NOTES:

1. Specified at recommended operating condition – see Table 1-2
2. Represents guaranteed VCO tuning range
3. Jitter tolerance, Jitter Generation with PRBS 2^{23}-1 or SMPTE color bar test pattern
4. Assume that reference is within +/-250ppm of desired data rate

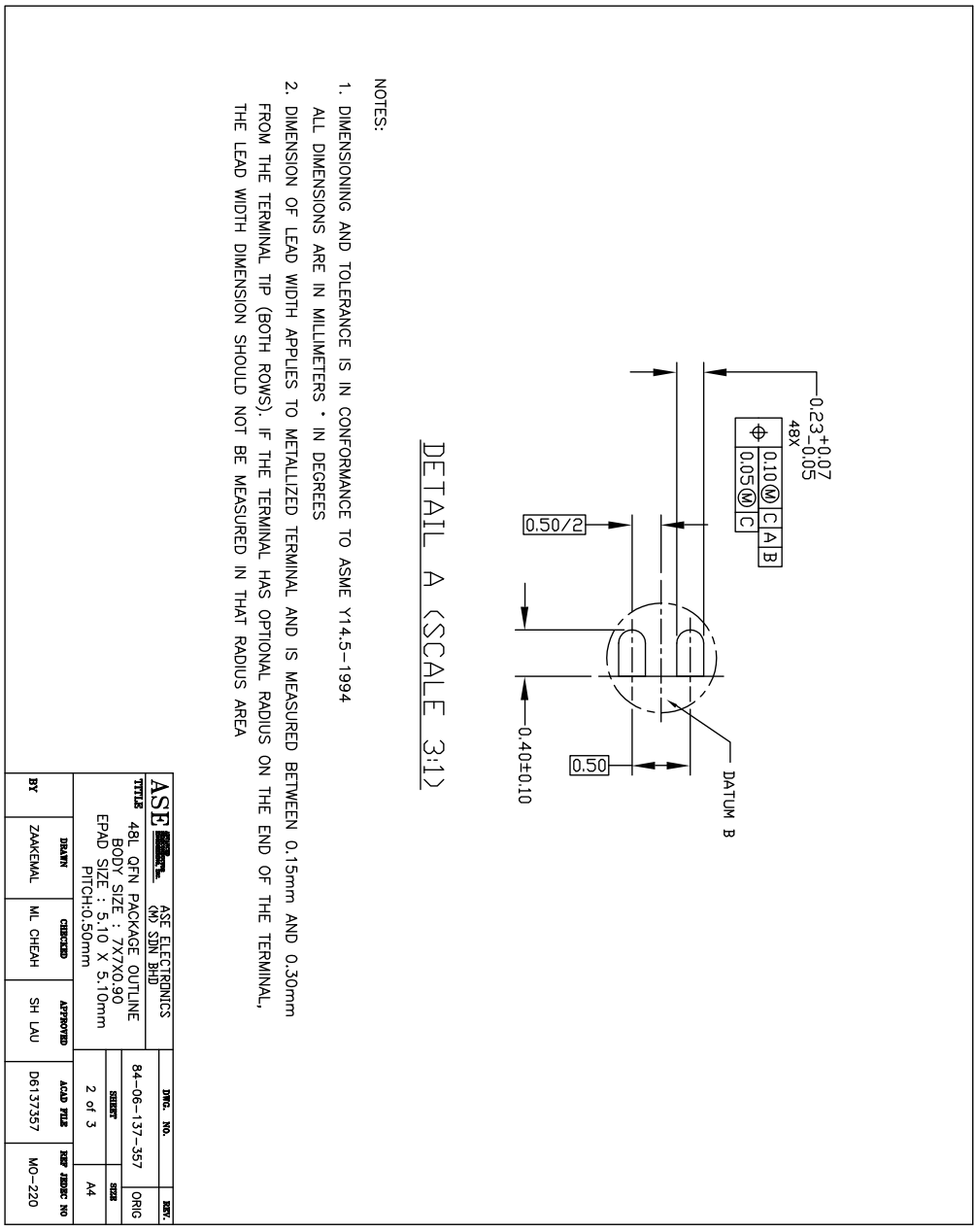
1.4 Package Specification

Figure 1-1. Package Drawing (1 of 2)



1. New ASE package and old Amkor package have the same footprint dimensions.

Figure 1-2. Package Drawing (2 of 2)



1. New ASE package and old Amkor package have the same footprint dimensions.

2.0 Functional Description

2.1 General Description

2.1.1 Reclocker General Overview

The reclocker is a dual loop based design. The primary phase locked loop (PLL) functions to 1) lock the VCO to the incoming data rate and 2) to retime the incoming data to remove jitter and is typically referred to as the clock and data recovery block (CDR). In general, the VCO tuning range for a multi-rate design is typically much larger than the frequency pull-in range of the CDR phase detector. As a result, a secondary frequency locked loop (FLL) is added to tune the VCO to the approximate data frequency so the CDR can lock onto valid data. The FLL uses an external crystal as an absolute frequency reference. As a result, the external reference is only used to assist the CDR frequency locking and the jitter performance of the reference has no effect on the recovered data output jitter.

2.1.2 Frequency Acquisition

In general, when the reclocker is out of lock (**$\overline{\text{LOL}}$** = Low), the FLL is enabled. The FLL then drives the VCO towards a frequency that is close to the incoming data rate frequency.

In principle, the FLL is shut off when the VCO approaches the data frequency. When FLL is shut off, **$\overline{\text{LOL}}$** = High, to indicate a lock condition. If valid data is present, then the CDR will lock to the incoming data. When in lock, the FLL control circuit continues to monitor the frequency difference between VCO and the reference and if the difference is too large, a loss of lock condition is indicated and frequency acquisition is initiated.

2.2 Pin Descriptions

2.2.1 General Nomenclature

Through out this data sheet, physical pins will be denoted in **bold** print. An array of pins can be called by each individual pin name (e.g. **MF0**, **MF1**, **MF2**, **MF3**, and **MF6**) or as an array (e.g. **MF[3:0, 6]**).

2.2.2 Pin Descriptions

Table 2-1. Control/Interface/Low-Speed Pins (1 of 3)

Pin Name	Pin #	Function	Default	Type
XTL_IN/$\overline{\text{XTL\_IN}}$	39, 40	Reference clock or crystal input. Upon power-up, this block defaults to the 14.140 MHz series resonance crystal. This can be changed to the 12.000 MHz parallel resonance crystal configuration through the appropriate software control register.	-	Analog Input
XTL_OUT/$\overline{\text{XTL\_OUT}}$	38, 37	Reference frequency output for chained reclocker applications.	-	O
IN_SEL[1:0]	14, 13	Input control signal that selects the active high-speed serial input. 00: Select **DDI0/$\overline{\text{DDI0}}$** 01: Select **DDI1/$\overline{\text{DDI1}}$** 10: Select **DDI2/$\overline{\text{DDI2}}$** 11: Select **DDI3/$\overline{\text{DDI3}}$**	Internal pull down	I-CMOS
MF4/ARD_EN	46	Input control signal that enables Auto Rate Detect (ARD) functionality or manual rate setting mode. **ARD_EN** = High: Auto Rate Detector (ARD) enabled **ARD_EN** = Low: Manual rate selection mode When the M21235 is in SW mode, this pin is used for Address 2 of the I^2C programming interface.	Internal pull up	I-CMOS
RATE[2:0]	18, 17, 16	Bidirectional control signals used to indicate the data rate in ARD enabled mode or to force a data rate setting in Manual mode. **ARD_EN** = High: **RATE[2:0]** pins indicate the date rate the M21235 is locked to according to pin decoding shown below: **ARD_EN** = Low: **RATE[2:0]** pins are used to force a particular data rate according to the pin decoding shown below: 000: 143 Mbps data rate 001: 177 Mbps data rate 010: 270 Mbps data rate 011: 360 Mbps data rate 100: 540 Mbps data rate 101: 1483.5/1485 Mbps data rate 111: Reclocker not locked and data is bypassed from input to output	Internal pull down	I/O-CMOS

Table 2-1. Control/Interface/Low-Speed Pins (2 of 3)

Pin Name	Pin #	Function	Default	Type
LOL	20	Output Status indication signal for reclocker Loss of Lock. See the Section 2.1.2, "Frequency Acquisition," on page 13 for more detailed information. **$\overline{\text{LOL}}$** = High: Reclocker PLL is locked **$\overline{\text{LOL}}$** = Low: Reclocker PLL is not locked	-	O-CMOS
SD/$\overline{\text{HD}}$	25	Output status indication signal to control slew rate of downstream cable driver. When the reclocker is unlocked, this pin defaults to LOW. **SD/$\overline{\text{HD}}$** = High: Reclocker locked to a SD data rate (143-540 Mbps) **SD/$\overline{\text{HD}}$** = Low: Reclocker locked to a HD rate (1.4835/1.485 Gbps)	-	O-CMOS
MF5/AUTO_BYPASS	47	Input control signal that automatically bypasses the data directly from the input to the output if the Reclocker PLL can NOT lock to the incoming data stream. **AUTO_BYPASS** = High: Auto bypass reclocker if lock is not achieved **AUTO_BYPASS** = Low: Reclocker continues to attempt data lock but output data BER may be high Address 3 of I^2C interface when device is in SW mode.	Internal pull up	I-CMOS
MF1/MAN_BYPASS	43	Input control signal used to force a reclocker PLL bypass regardless of the setting of the AUTO_BYPASS signal. **MAN_BYPASS** = High: Force bypass (regardless of **AUTO_BYPASS** state) **MAN_BYPASS** = Low: Enables normal **AUTO_BYPASS** operation SDA for the I^2C interface when device is in SW mode.	Internal pull up	I- CMOS
MF2/LBW_INC[0]	26	Input control signal used to increase the Loop Bandwidth from the nominal setting. **LBW_INC[0]** = High or Floating: Normal operation **LBW_INC[0]** = Low: Increased bandwidth Address 0 of I^2C interface when device is in SW mode.	Internal pull up	I-CMOS
MF3/LBW_INC[1]	45	Input control signal that can be used to increase LBW. Refer to Table 2-4. **LBW_INC[1]** = High: Normal LBW (floating default) **LBW_INC[1]** = Low: Increased bandwidth Address 1 of I^2C interface when device is in SW mode.	Internal pull up	I-CMOS
OUTMODE[1:0]	23, 30	In HW mode, selects the type of output mode (reserved for future use). 00: CML output 01: Reserved 10: Reserved 11: Reserved	Internal pull up	I-CMOS

Table 2-1. Control/Interface/Low-Speed Pins (3 of 3)

Pin Name	Pin #	Function	Default	Type
OUTMODE[3:2]	22, 29	In HW mode, selects the swing for the high-speed output buffers. 00: Power down 01: 500 mV 10: 800 mVpp 11: 1600 mV	Internal pull up	I-CMOS
MF6	48	Address 4 of the I^2C interface when device is in SW mode.	Internal pull up	I-CMOS
MF0	42	SCL for the I^2C interface when device is in SW mode.	Internal pull up	I-CMOS
$\overline{\text{RST}}$	24	Hardware reset pin. Need to pull down to issue reset.	Internal pull up	I-CMOS
MODESET	28	HW/SW Mode Select pin: **MODESET** = High: HW control mode **MODESET** = Low: SW control mode	Internal pull up	I-CMOS
NOTE: Internal pull-up or pull-down resistance is 100 kΩ (typical).				

Table 2-2. Power Pins

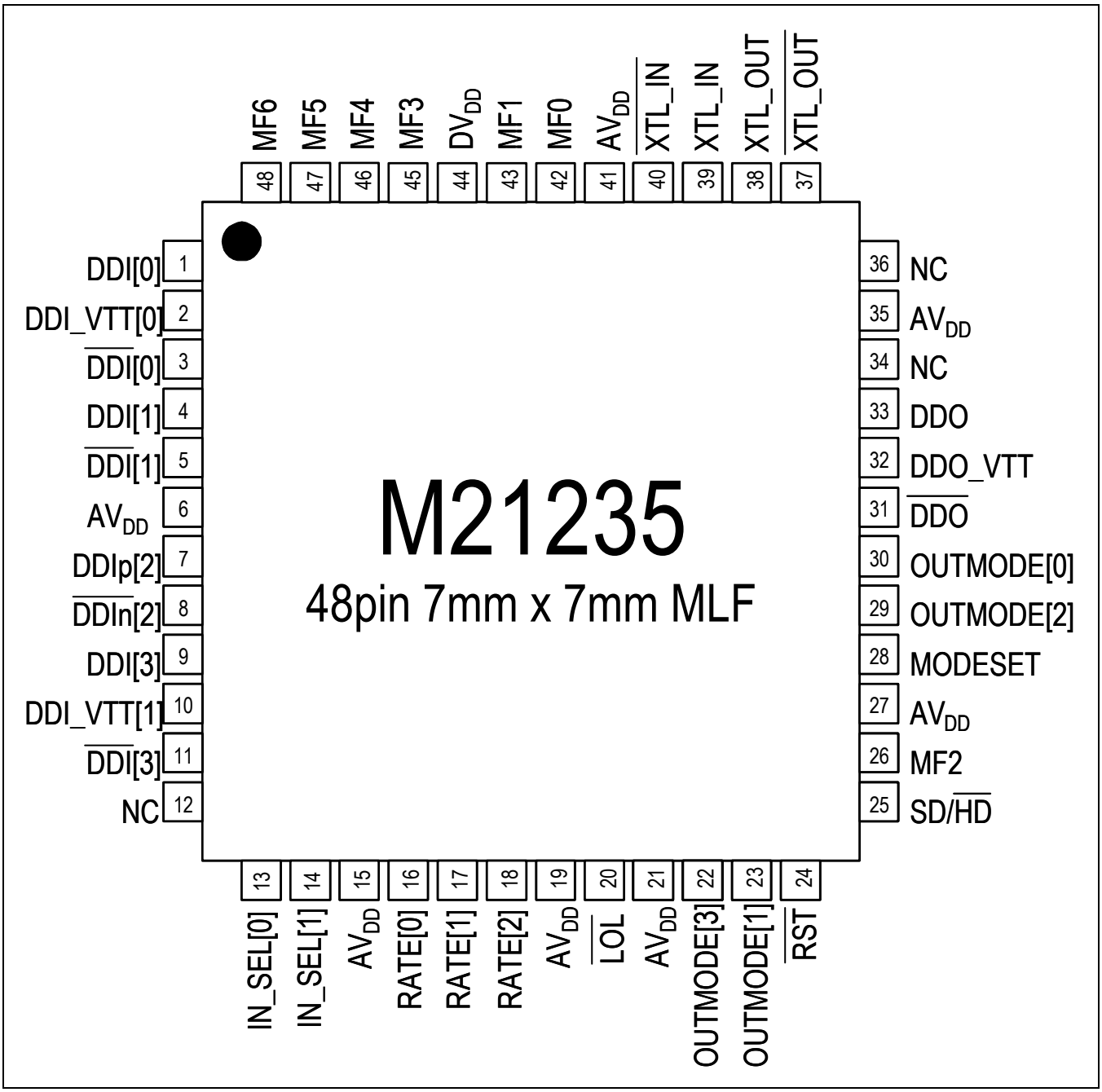
Pin Name	Pin #	Function	Type
V_{SS}	PAD	Chip Ground. Paddle must be soldered to PCB using an array of thermal vias.	Power
AV_{DD}	6, 15, 19, 21, 27, 35, 41	Power Supply.	Power (Analog)
DV_{DD}	44	Power Supply.	Power (Digital)

Table 2-3. High-speed Signal Pins

Pin Name	Pin #	Function	Default	Type
DDI/$\overline{\text{DDI}}$[3:0]	1, 3, 4, 5, 7, 8, 9, 11	Internally terminated. Non-inverting and inverting high speed serial data inputs.	100Ω differential	I-High-speed
DDI_VTT[1:0]	2,10	Input termination pin (center tap for 50Ω). Case 1: Tie to a positive supply for 50Ω to supply terminal Case 2: Leave floating and decouple to gnd for 100Ω differential		Term
DDO/$\overline{\text{DDO}}$	33, 31	Internally terminated. Non-inverting and inverting high speed serial data outputs.	100Ω differential	O-High-speed
DDO_VTT	32	Output termination center tap. Tie to a positive supply for 50Ω to supply termination.		Term

The M21235 is available in a 48-pin 7 mm x 7 mm MLF package. The pin out is shown in Figure 2-1 and the package drawing in Figure 1-1 and Figure 1-2. Regular (with Pb) or RoHS compliant options available.

Figure 2-1. M21235 Pin Out



2.2.2.1 Power/Reset

The M21235 is designed to work at an extended power supply range from 1.8 to 3.3V for further reduction of power and to simplify the interface to the next generation of ASICs. The M21235 reclocker automatically resets after power up thus an external reset is not required. The M21235 is fully operational 10 ms after the power supply has stabilized to within 10% of the final value. An external hardware reset pin **$\overline{\text{RST}}$** is provided for manually resetting the device or it may be reset through the control register using the I^2C interface.

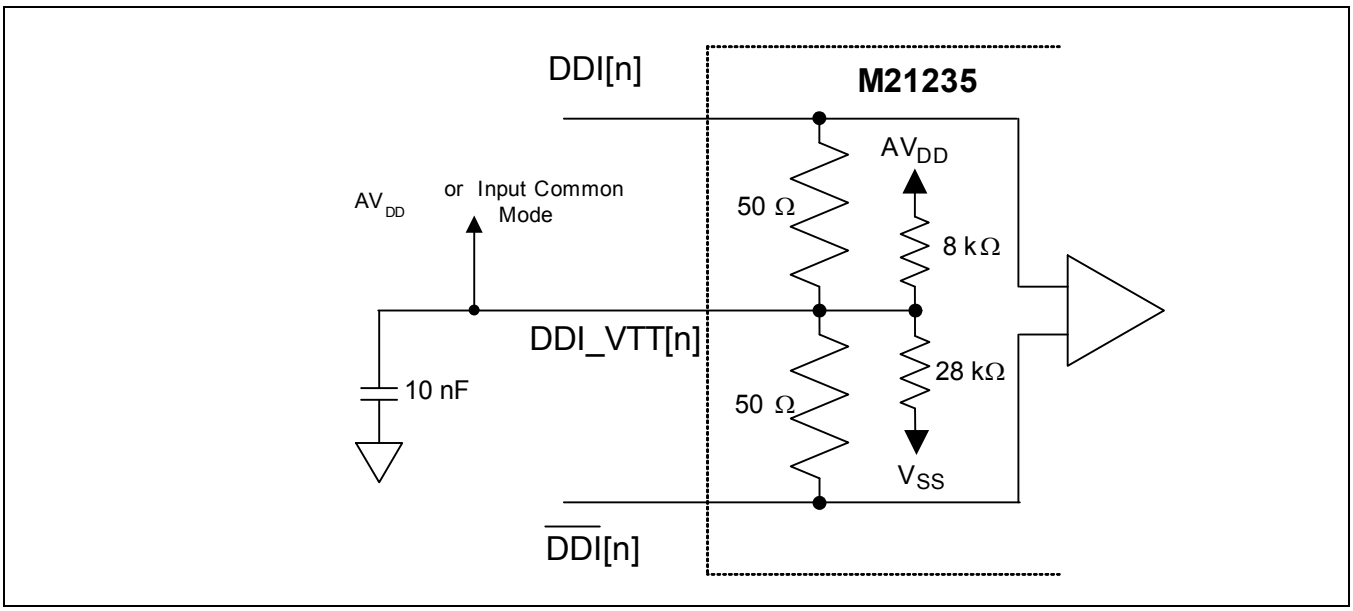
2.2.2.2 Input Selection Multiplexer

The M21235 contains a 4:1 input selection multiplexer. The **IN_SEL[1:0]** pins select one of the four possible inputs that will be retimed by the reclocker block and passed to the output. The mapping of the multiplexer pin is shown in Table 2-1. If the **IN_SEL[1:0]** pins are left floating, the 4:1 input multiplexer defaults to input **DDI[0]/$\overline{\text{DDI[0]}}$.**

2.2.2.3 High-Speed I/O Pins

The high-speed inputs are designed to be used in both AC coupled and DC coupled modes. The high-speed differential inputs contain on-chip 50Ω termination from **DDI[n]** to **DDI_TERM[n]** as well as from **DDI[n]** to **DDI_VTT[n]**. Figure 2-2 shows the recommended connection of the **DDI_VTT[n]** pin for AC coupled inputs or with DC coupled CML when the CML is driven from the same supply voltage. For use in other DC coupled situations, it is recommended that the termination voltage for the M21235 be set at the input common mode level and that the common mode and input swing falls within the specified range as shown in Table 1-5. **DDI_TERM[n]** contains a weak internal bias near **AV_{DD}**, and should be decoupled to **V_{SS}** to reduce input noise with a 10 nF capacitor.

Figure 2-2. Input circuit for M21235



The high-speed output contains integrated 50Ω resistors from both **DDO** and **$\overline{\text{DDO}}$** to **VDDO_TERM**. **VDDO_TERM** should be bypassed to **V_{SS}** with a 10nF capacitor. **VDDO_TERM** is internally biased to **AV_{DD}**.

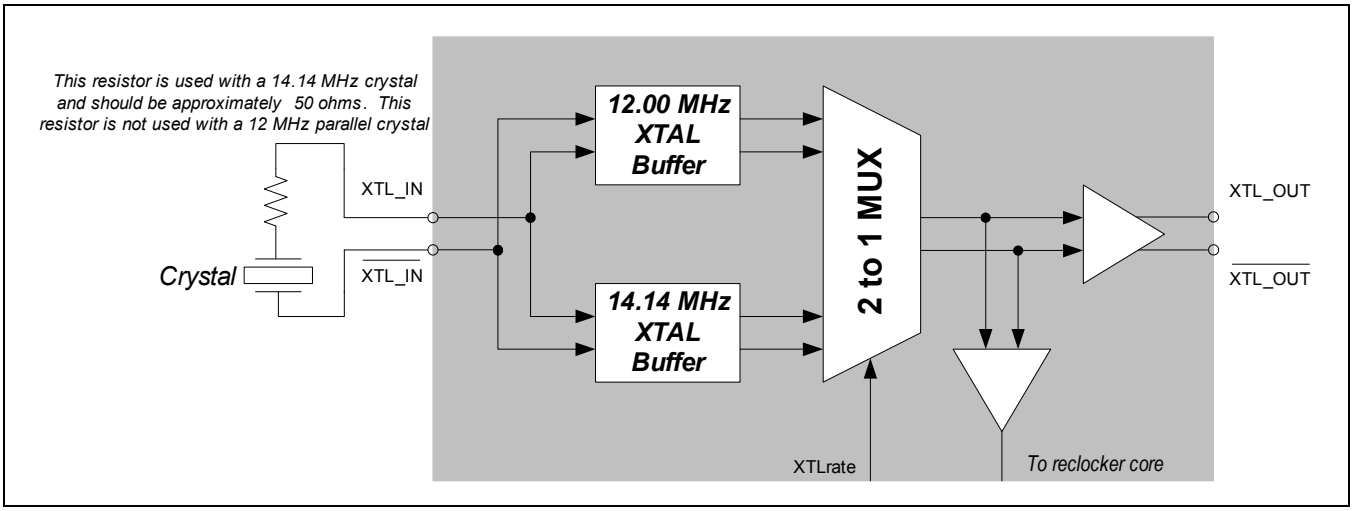
2.2.2.4 Reclocker Reference Frequency

The reclocker frequency acquisition requires an external frequency source applied to **XTL_IN/XTL_IN**. The M21235 reference input can be a standard crystal, a crystal oscillator with CMOS/TTL single ended outputs, or a differential PCML/LVDS/LVPECL system clock. For daisy-chained reclocker applications, a buffered reference output is made available on **XTL_OUT/XTL_OUT**.

The input reference frequency can be either 12.000 MHz or 14.140 MHz. By default, the M21235 expects a 14.140 MHz series resonance crystal. The M21235 can also be used with a 12.000 MHz parallel resonance reference crystal which was selected based on the SD/HD-SDI bitrates as well as the fact that the 12.000 MHz is a common-stocked low cost standard rate crystal. A 56Ω resistor is recommended for the series resonance case and the series resistor is set to 0 ohms for the 12.00 MHz parallel resonance crystal. Bits[5:4] of register address 08h are used to configure the M21235 to operate with a parallel or series crystal.

When a 14.14 MHz series or 12.00 MHz parallel resonant crystal is used with the M21215, the crystal should be connected as shown in Figure 2-3 below.

Figure 2-3. Application circuit when a series or parallel resonant crystal is used



The series resonant crystal should operate at 14.14 MHz with a frequency stability of +/- 50 ppm or better, equivalent series resistance of 80Ω or less, drive level of < 0.2 mW, and static capacitance of less than 5.0 pF. The parallel resonant crystal should operate at 12.00 MHz with a frequency stability of +/- 50 ppm or better, equivalent series resistance of 80Ω or less, drive level of < 0.2 mW, and static capacitance of less than 5.0 pF.

The M21235 can also operate with a reference from an external clock buffer or oscillator instead of a crystal. The M21235 can accept a single ended or differential 14.14 MHz reference clock, and a single ended 12.00 MHz reference clock. When driving the M21235 with a single ended reference clock, the clock signal should be connected to the **XTL_IN** pin and the **XTL_IN** pin should be left floating. If a 14.14 MHz reference clock is used, the ***XTAL_MODE* [1:0]** bits should be set to '11', and if a 12.00 MHz reference clock is used, the ***XTAL_MODE* [1:0]** bits should be set to '10'. If the **XTL_IN** pins on the M21235 are connected to a clock driver or oscillator, the requirements for the signal connected to the M21235 are detailed in Table 1-7.

By default 14.140MHz operation is used.

2.2.2.5 Reclocker Loop Bandwidth

For SD-SDI rates, the loop bandwidth scales proportionately to the bit rate, using the 270 Mbps as a reference point. For example, at 540 Mbps, the bandwidth is 2x the 270 Mbps bandwidth. When **LBW_INC[0]** = Low, the bandwidth increases to 3.5 MHz for 1485 Mbps data rates and 1 MHz for 270 Mbps data rates.

For improved synchronous lock time, the M21235 offers a still higher loop bandwidth option of 5 MHz for 1485 Mbps data rates and 1.4 MHz for 270 Mbps data rates when **LBW_INC[0]** and **LBW_INC[1]** =Low.

Table 2-4. Loop Bandwidth Control Setting (in H/W control mode)

LBW_INC[1]	LBW_INC[0]	LOOP BANDWIDTH (1,485 Mbps)	LOOP BANDWIDTH (270 Mbps)
0	0	5.0 MHz	1.4 MHz
0	1	5.0 MHz	1.4 MHz
1	0	3.5 MHz	1.0 MHz
1	1	1.5 MHz (default)	520 KHz (default)
NOTE: Scales to lower frequency with reduced data rates.			

2.2.2.6 Loss of Lock Alarm

A loss of lock alarm pin, **$\overline{\text{LOL}}$**, is provided to indicate if the reclocker is in lock. When the reclocker has achieved lock, **$\overline{\text{LOL}}$** = High. If the reclocker is out of lock, **$\overline{\text{LOL}}$** = Low. For synchronous switching at the same data rate, the lock time is lower if a higher loop bandwidth is selected.

2.2.2.7 Auto Rate Detect (ARD)

The M21235 is designed to operate in two modes. In the first mode, with **ARD_EN** = High, the Auto Rate Detect is enabled which automatically locks the CDR to the rates typically used in SD-SDI, HD-SDI, and DVB-ASI applications. The locked to data rate is then reported with **RATE[2:0]** pins as shown in Table 2-5.

With the ARD disabled (**ARD_EN** = Low), the reclocker locking frequency is forced by using the **RATE[2:0]** pins as inputs and selecting the data rate as shown in Table 2-6. In this case, there are two additional non-standard rates that are supported by the M21235 part.

Table 2-5. Rate Report Mapping when ARD is Enabled

RATE[2:0]	Bit Rate
000	143 Mbps
001	177 Mbps
010	270 Mbps
011	360 Mbps
100	540 Mbps
101	1485/1483.5 Mbps
111	Unlocked

Table 2-6. Rate Select with ARD Disabled

RATE[2:0]	Bit Rate
000	143 Mbps
001	177 Mbps
010	270 Mbps
011	360 Mbps
100	540 Mbps
101	1485/1483.5 Mbps
110	Non-standard 140 Mbps
111	Non-standard 155 Mbps

For system reporting purposes as well as to set the output slew rate on the cable drivers, the **SD/$\overline{\text{HD}}$** output is used to indicate if the reclocker has locked to a HD rate. For SD-SDI rates, **SD/$\overline{\text{HD}}$** = High and for the HD-SDI rate **SD/$\overline{\text{HD}}$** =Low.

To improve on the asynchronous lock times, the M21235 offers several options with the ARD algorithm.

177lockout = High would remove the 177 Mbps rate from the search sequence resulting in a slightly faster asynchronous lock time but as there are not any false locking issues with DVB-ASI with the M21235 this is not required.

Also, if the M21235 is out-of-lock, the search pattern will not start unless the M21235 detects that there are transitions in the data through an internal loss of signal detector. To reduce the lock time even further, the M21235 offers several alternative ARD search sequences that are set with the **ARD_FN[1:0]** register control bits and these are summarized in Table 2-7.

Table 2-7. ARD Search Patterns Selections

ARD_FN[1:0]	M21235 Additional ARD Search Sequences
11 (default)	start->143->177->270->360->540->1483.5/1485->repeat
10	start->270->360->540->1485/1483.5->repeat
01	start->270->360->1485/1483.5->repeat
00	start->270->1485/1483.5->repeat

2.2.2.8 Bypass and $\overline{\text{DDO\_MUTE}}$

The reclocker can be forced into the bypass mode (input data to output without retiming) with **MAN_BYPASS** = High. With **MAN_BYPASS** = Low (normal operation), **AUTO_BYPASS** = High enables the auto bypass mode that puts the reclocker into the bypass mode whenever **LOL** = Low (i.e. the reclocker is out of lock).

This implies that if both **MAN_BYPASS** and **AUTO_BYPASS = Low**, when the reclocker is not in lock, unlocked data will appear at the output. This mode may be used for troubleshooting or debug purposes.

When the reclocker is not in a bypass state, the output can be forced to a logic low with **$\overline{\text{DDO\_MUTE}}$** = Low. This function can be used to squelch the noise output.

Table 2-8. Manual and Auto Bypass Setting

MAN_BYPASS	AUTO_BYPASS	Functional Description
0	0	Retimed Reclocker Output
0	1	Bypass if Reclocker out of lock
1	0	Forced Bypass
1	1	Forced Bypass

To prevent the propagation of noise in the case where there is an LOL condition, the RCLK contains an auto-inhibit feature, which is enabled by setting bit 3 (autoinh_en) in Reclocker Control A register to a logic 1. When LOL is active, the output at DDO is fixed at a logic low state. By default this feature is disabled.

2.2.3 Two-Wire Serial Interface

The two-wire serial interface is compatible with the I^2C standard. The M21235 supports the read/write slave-only mode, 5-bit device address field width, and supports the standard rate of 100 Kbps, fast mode of 400 Kbps, and high-speed mode of 3.4 Mbps. The 5-bit address for the device is determined with **MF [6:2]**, which allows for a maximum of 32 unique addresses for this device. SDA (**MF1**) and SCL (**MF0**) can drive a maximum of 500 pF each at the maximum rate. During the write mode from the master to the M21235, data is latched into the internal M21235 registers on the rising edge of SCL, during the acknowledge phase (ACK) of communication. Table 2-9 summarizes the multifunction pins for the two-wire serial interface mode. For further information on timing, please see the I^2C bus specification standard.

Table 2-9. Multifunction Pins for Two-Wire Interface in SW Control Mode

Pin	Function	Description
MF0	SCL	Clock input (open drain)
MF1	SDA	Data input/output (open drain)
MF2	Address bit 0	5-bit device address; address bit 0 is LSB
MF3	Address bit 1	5-bit device address; address bit 1
MF4	Address bit 2	5-bit device address; address bit 2
MF5	Address bit 3	5-bit device address; address bit 3
MF6	Address bit 4	5-bit device address; address bit 4 is MSB

Table 2-10. Multifunction Pins in HW Control Mode

Pin	Function	Description
MF0	N/C	Not used in HW mode.
MF1	Manual Bypass	Used to force reclocker into bypass mode.
MF2	LBW_INC[0]	Used to increase the loop bandwidth. Refer to Table 2-4.
MF3	LBW_INC[1]	Used to increase the loop bandwidth. Refer to Table 2-4.
MF4	ARDEN	Used to enable Auto Rate Detect functionality.
MF5	Auto Bypass	Used to force reclocker into bypass mode when out of lock.
MF6	Vss	Connect to Vss in HW mode.

3.0 Registers

3.1 Register Map

Table 3-1. Register Summary

Addr	Register Name	d7: MSB	d6	d5	d4	d3	d2	d1	d0: LSB	Register Default
Common Registers										
00h	mastreset	rst	rst	rst	rst	rst	rst	rst	rst	00h
01h	chipcode	chipcode[7]	chipcode[6]	chipcode[5]	chipcode[4]	chipcode[3]	chipcode[2]	chipcode[1]	chipcode[0]	77h
02h	revcode	revcode[7]	revcode[6]	revcode[5]	revcode[4]	revcode[3]	revcode[2]	revcode[1]	revcode[0]	22h
Reclocker Registers										
03h	RCLK_ctrlA	softreset	Clear_alarm	RSVD	RSVD	autoinh_en	RSVD	RSVD	RSVD	87h
04h	RCLK_ctrlB	RSVD	RSVD	RSVD	BW[1]	BW[0]	RSVD	RSVD	MAN_bypass	44h
06h	RCLK_ctrlD	RSVD	RSVD	ARDen	ARD_FN[1]	ARD_FN[0]	RATE_SEL[2]	RATE_SEL[1]	RATE_SEL[0]	3Dh
07h	RCLK_ctrlE	RSVD	RSVD	RSVD	$\overline{\text{DDO\_MUTE}}$	177lockout	autobypass	Insel[1]	Insel[0]	74h
08h	Xtal_ctrl	RSVD	RSVD	Xtal_mode[1]	Xtal_mode[0]	RSVD	RSVD	RSVD	RSVD	35h
0Ah	Dout_ctrlB	RSVD	RSVD	RSVD	RSVD	Out_lvl[1]	Out_lvl[0]	Out_mode[1]	Out_mode[0]	3Ch
0Eh	los_ctrl	RSVD	RSVD	RSVD	LOS_DISABLE	RSVD	Los_lvl[2]	Los_lvl[1]	Los_lvl[0]	40h
13h	alarm_reg (LH)	SDxHD	RSVD	lol	RSVD	RSVD	RSVD	RSVD	los	N/A
14h	RATE	RSVD	RATE[2]	RATE[1]	RATE[0]	RSVD	RSVD	RSVD	RSVD	N/A

Register Table Details:

1. Do not write to undefined register addrsses – operation not guaranteed.
2. RSVD Internal: Defines register bits for MACOM use only: Must always write the default value MPSD internal bits. When in doubt, read back default value after reset.

3.2 Register Tables

3.2.1 Master Chip Reset

Table 3-2. Master Chip Reset (mastreset: Address 00h)

Bits	Type	Default	Label	Description
7:0	W	0h	rst	Same feature has hardware ***RST***. Resets entire IC. (Write only) AAh: Reset upon write to this register with AAh. 00h: Normal operation All other values are ignored.

3.2.2 Chip Electronic ID

Table 3-3. Chip Electronic ID (chipcode: Address 01h)

Bits	Type	Default	Label	Description
7:0	R	77h	chipcode	This read only register contains the ID of this device.

3.2.3 Chip Revision Code

Table 3-4. Chip Revision Code (RevCode: Address 02h)

Bits	Type	Default	Label	Description
7:0	R	24h	revcode	This read only register contains the revision of the part. Format is A.B where A is the main rev and B is the sub rev Default value is 22h for Rev 1.0

3.2.4 Reclocker Control - A

Table 3-5. Reclocker Control - A (RCLK_ctrlA: Address 03h)

Bits	Type	Default	Label	Description
7	R/W	1	softreset	Resets the reclocker only (Setup registers remain unchanged, need to softreset after rate change) 0: Reset RCLK only 1: Normal Operation
6	R/W	0	clear_alarm	Clear alarm registers 0: Normal Operation 1: Clear all alarm registers, see Table 3-12
5	R/W	0	RSVD	For MACOM use only. Must be set to 0
4	R/W	0	RSVD	For MACOM use only. Must be set to 0
3	R/W	0	autoinh_en	Autoinhibit enable 0: Autoinhibit disabled 1: Inhibit data output to low when reclocker issues an out of lock or loss of signal alarm
2	R/W	1	RSVD	For MACOM use only. Must be set to 1
1	R/W	1	RSVD	For MACOM use only. Must be set to 1
0	R/W	1	RSVD	For MACOM use only. Must be set to 1

3.2.5 Reclocker Control Register - B

Table 3-6. Reclocker Control Register - B (RCLK_ctrlB: Address 04h)

Bits	Type	Default	Label	Description
7:5	R/W	010	RSVD	For MACOM use only. Must be set to 010b.
4:3	R/W	00	LBW_INC[1:0]	Nominal Loop BW control 00: HD: BW = 1.5 MHz, SD @ 270 MHz BW = 0.52 MHz 01: HD: BW = 3.5 MHz, SD @ 270 MHz BW = 0.52 MHz 10: HD BW = 5.0 MHz, SD @ 270 Mhz BW = 1.0 MHz 11: HD BW = 5.0 MHz, SD @ 270 MHz BW = 1.4 MHz
2	R/W	1	RSVD	For MACOM use only. Must be set to 1
1	R/W	0	RSVD	For MACOM use only. Must be set to 0
0	R/W	0	MAN_BYPASS	Forces the reclocker to bypass the input to the output without retiming 0: Normal operation (Retimed data out) 1: Force Bypass

3.2.6 Reclocker Control Register - D

Table 3-7. Reclocker Control Register - D (RCLK_ctrlD: Address 06h)

Bits	Type	Default	Label	Description
7:6	R/W	00	RSVD	For MACOM use only. Must be set to 00b.
5	R/W	1	ARD_EN	Auto rate detection enable/disable 0: Auto rate detect OFF 1: Auto rate detect ON
4:3	R/W	11	ARD_FN[1:0]	Sets the ARD search order and bit rate (repeated) 00: 270 -> 1485Mb/s 01: 270 -> 360 -> 1485 Mb/s 10: 270 -> 360 -> 540 -> 1485 Mb/s 11: 143 -> 177 -> 270 -> 360 -> 540 -> 1485 Mb/s
2:0	R/W	101	RATE_SEL[2:0]	Data rate information for manual HW mode (**ARD_EN**=0) 000: 143 Mb/s 001: 177 Mb/s 010: 270 Mb/s 011: 360Mb/s 100: 540Mb/s 101: 1483.5/1485b/s 110: 140 Mb/s 111: 155 Mb/s **Note**: Used to manually force a given data rate.

3.2.7 Reclocker Control Register - E

Table 3-8. Reclocker Control Register - E (cdr_ctrlE00: Address 07h)

Bits	Type	Default	Label	Description
7:5	R/W	011	RSVD	For MACOM use only. Must be set to 011b
4	R/W	1	DDO_MUTE	Inhibit data outputs 0: Inhibit to low 1: Normal mode
3	R/W	0	177lockout	Disable 177Mb/s rate from auto detection circuit 0: Do not disable 177Mb/s rate from auto detection circuit 1: Disable 177Mb/s rate from auto detection circuit
2	R/W	1	AUTO_BYPASS	Bypass reclocker when out of lock 0: Do not bypass when out of lock 1: Bypass reclocker when out of lock
1:0	R/W	00	IN_SEL[1:0]	Input channel select IN_SEL[1:0]Input Channel Selected 00SDI [0] 01SDI [1] 10SDI [2] 11SDI [3]

3.2.8 Crystal Oscillator Control

Table 3-9. Crystal Oscillator Control (Xtal_ctrl: Address 08h)

Bits	Type	Default	Label	Description
7:6	R/W	00	RSVD	For MACOM use only. Must be set to 00b
5:4	R/W	11	xtal_mode[1:0]	Reclocker reference clock modes 00: Power down XTAL oscillators 01: Parallel mode XTAL oscillator (12.00MHz) ON 10: Bypass XTAL oscillators, apply external clock 11: Serial mode XTAL oscillator ON (14.14MHz)
3:0	R/W	0101	RSVD	For MACOM use only. Must be set to 0101.

3.2.9 Data Output Control - B

Table 3-10. Data Output Control - B (DoutCtrlB: Address 0Ah)

Bits	Type	Default	Label	Description
7:4	R/W	0011	RSVD	For MACOM use only. Must be set to 0010b
3:2	R/W	11	out_lvl[1:0]	Setting Swing 00: Power down 0 mV 01: Low swing 500 mV 10: Medium swing 800 mV (LVDS) 11: High swing 1600 mV
1:0	R/W	00	out_mode[1:0]	Output buffer mode 00: CML 01: Reserved 10: Reserved 11: Reserved

See Table 1-6 for details.

3.2.10 Loss of Signal (LOS) Control

Table 3-11. Loss of Signal (LOS) Control (Los_ctrl: Address 0Eh)

Bits	Type	Default	Label	Description
7:5	R/W	010	RSVD	For MACOM use only. Must be set to 010
4	R/W	0	LOS_DISABLE	Enable/Disable LOS detection circuit 0: LOS detection enabled 1: LOS detection disabled
3	R/W	0	RSVD	For MACOM use only. Must be set to 0
2:0	R/W	000	los_lvl[2:0]	LOS threshold level 000: 40mV 001: 50mV 010: 60mV 011: 70mV 100: 20mV 101: 30mV 110: Not used 111: Not used

3.2.11 Alarm Register (Read Only)

Table 3-12. Alarm Register (Alarm_Reg[LH]: Address 13h)

Bits	Type	Default	Label	Description
7	R	N/A	SD/$\overline{HD}$	SD/HD rate monitor 0: HD rate 1: SD rate
6	R	N/A	RSVD	For MACOM use only.
5	R	N/A	LOL	Loss of Lock Monitor 1: LOL alarm asserted 0: LOL alarm de-asserted
4:1	R	N/A	RSVD	For MACOM use only.
0	R	N/A	LOS	Loss of signal indication 1: LOS alarm asserted 0: Los alarm de-asserted Note: Indicates LOS condition on selected input channel.
NOTE: Latches alarm on L-to-H transition. Use Clear Alarm bit in 03h register bit 6 to clear all alarms.				

3.2.12 Status Register (Read Only)

Table 3-13. Rate Code (Rate_trim: Address 14h)

Bits	Type	Default	Label	Description
7	R	N/A	RSVD	For MACOM use only.
6:4	R	N/A	RATE_IND [2:0]	Rate information Indication when ARD_EN = 1 000: 143 Mb/s data rate 001: 177 Mb/s data rate 010: 270 Mb/s data rate 011: 360 Mb/s data rate 100: 540 Mb/s data rate 101: 1483.5/1485 Mb/s data rate 110: Invalid 111: Reclocker not locked
3:0	R	N/A	RSVD	For MACOM use only.

Appendix

A.1 Glossary of Terms/Acronyms

ARD	Automatic Rate Detection
BER	Bit Error Rate
CD	Cable Driver
CDA	Cable Distribution Amplifier
CML	Current Mode Logic
DDI	Differential Data Inputs
DPLL	Digital Phase Locked Loop
DTV	Digital Television
DVB	Digital Video Broadcast
EMI	Electro Magnetic Interference
EQ	Equalizer or Equalization
ESD	Electro Static Discharge
GREEN	Environmentally friendly
HD	High Definition
HW	Hardware
ID	Identifier
I^2C	Inter-IC Communication (2 wire serial control bus)
I/O	Input/Output
LVPECL	Low Voltage Positive Emitter Coupled Logic
MLF	Micro Lead Frame package (also called QFN)
PHY	Pertaining to the Physical Layer of the OSI Model
SD	Standard Definition
SDI	Serial Digital Input
SDO	Serial Digital Output

SE	Single Ended
SMPTE	Society of Motion Picture and Television Engineers
SOIC	Small Outline Integrated Circuit
SW	Software

A.2 Reference Documents

A.2.1 External

The following external documents were referenced in this data sheet.

- The I^2C Bus Specification version 2.1
- SMPTE 292M, SMPTE 259M, SMPTE 344M
- ESI TR101 891 DVB Asynchronous Serial Interface (ASI)