AK4617

192kHz 24-bit 2ch/12ch Audio CODEC

1. General Description

The AK4617 is a single chip audio CODEC that includes 2-channel ADC and 12-channel DAC. The stereo ADC supports differential/single-ended analog inputs. The high performance 12-channel DAC integrates full-range digital volume control and achieves 106dB dynamic range. A car audio system can be easily designed with an audio DSP and the AK4617. The AK4617 is housed in a space saving 48-pin LQFP package.

2. Features

- **2ch ADC**
  - **Sampling Frequency: 8kHz~48kHz**
  - **ADC S/N: 97dB, S/ (N+D): 87dB**
  - **I/F format: MSB justified, I^2S or TDM**
- **12ch DAC**
  - **Sampling Frequency: 8kHz~192kHz**
  - **DAC S/N: 106dB, S/ (N+D): 85dB**
  - **I/F format: MSB justified, LSB justified (16bit, 24bit), I^2S or TDM**
- **Channel Independent Digital Attenuator (Linear 256 steps)**
- **Master / Slave mode**
- **Master clock**
  - **Slave mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=8kHz ~ 48kHz)**
    256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
    128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
  - **Master mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=8kHz ~ 48kHz)**
    256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
    128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
- **µP I/F: I^2C or 3-wire**
- **Power supply**
  - **Analog Power Supply: 3.0V ~ 3.6V (typ.3.3V)**
  - **Digital I/O Power Supply: 3.0V ~ 3.6V (typ.3.3V)**
- **Operating temperature range: -40°C ~ 105°C**
- **Package: 48pin LQFP**

3. Table of Contents

4. Block Diagram and Functions

■ Block Diagram

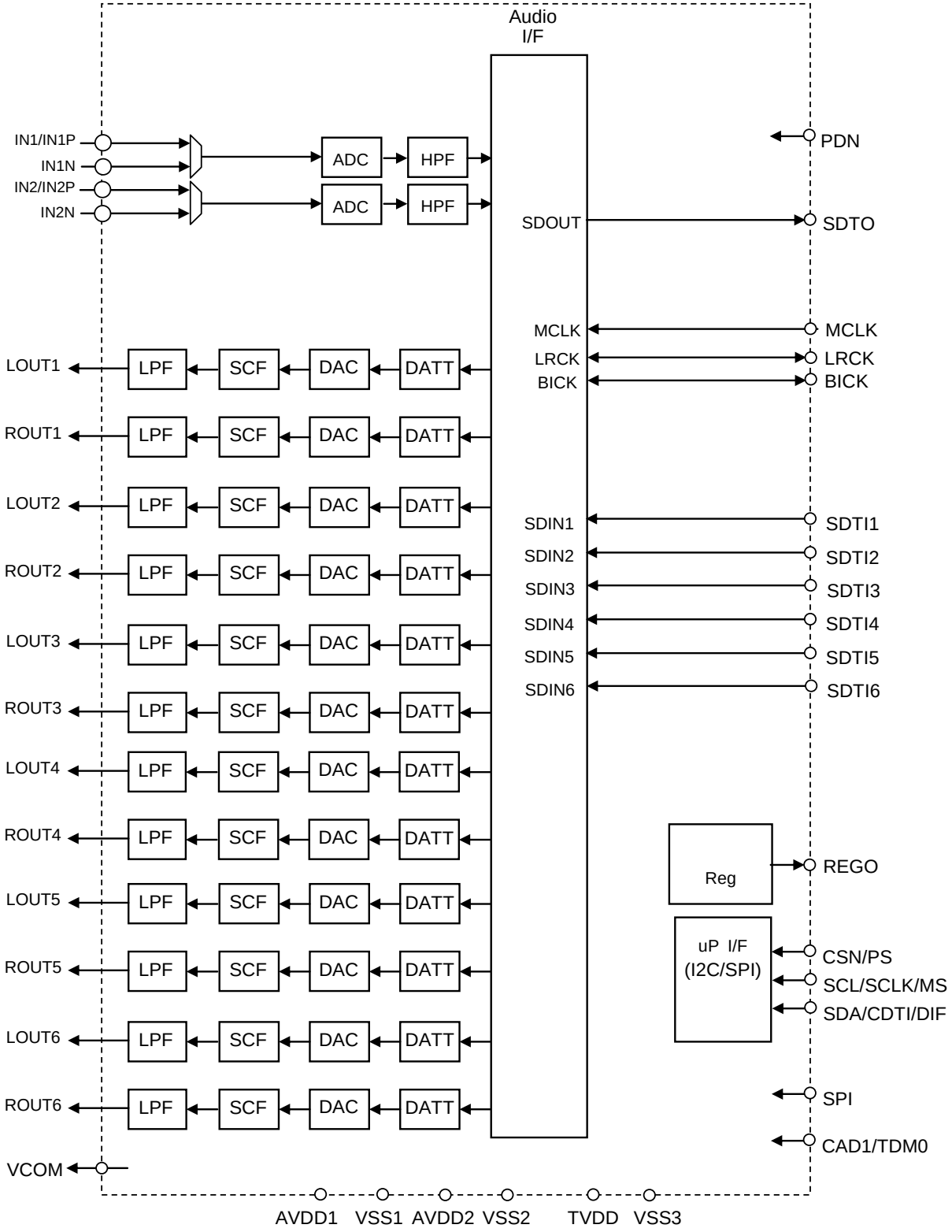
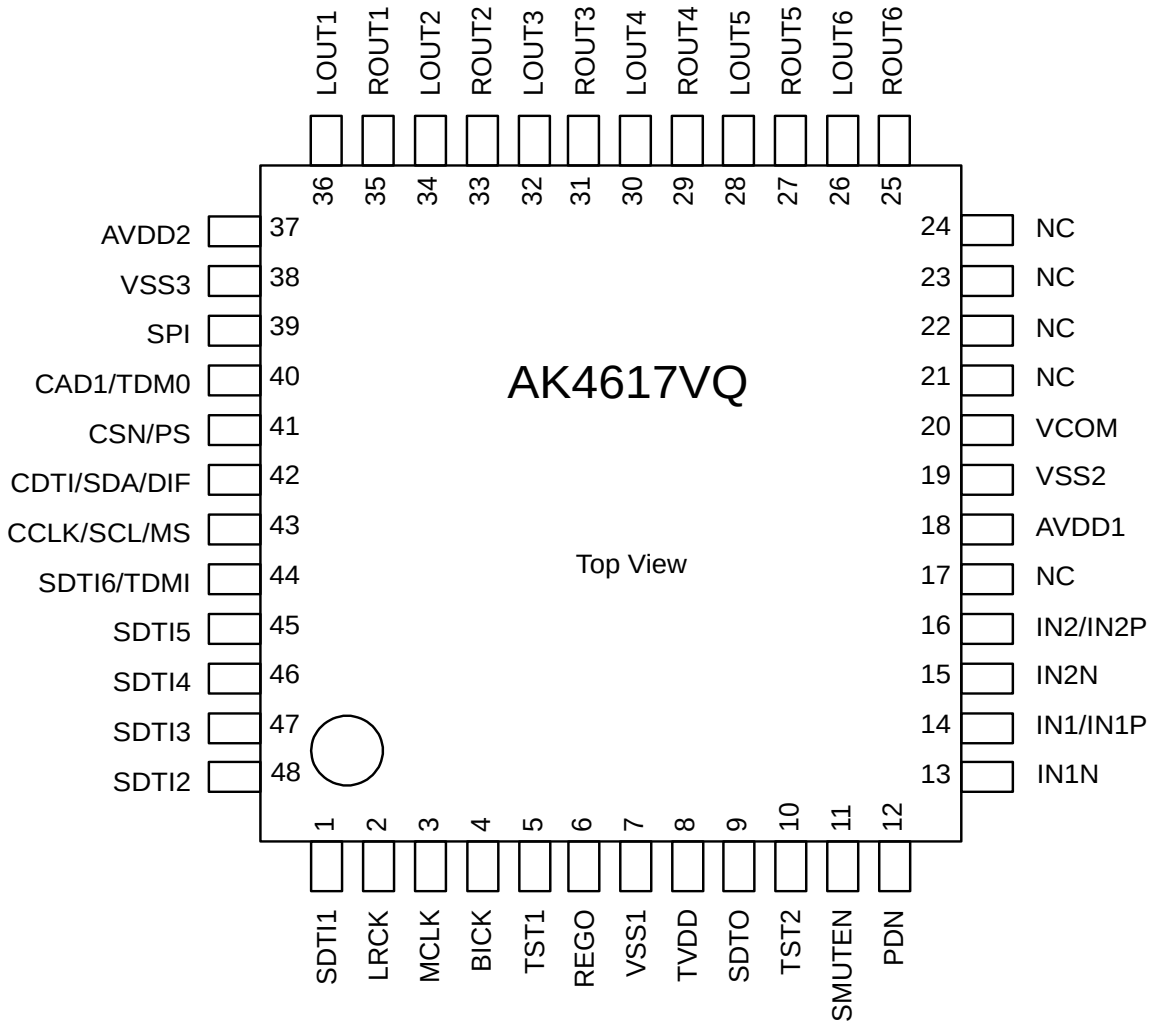


Figure 1. Block Diagram

■ Ordering Guide

AK4617VQ	–40 ~ +105°C	48pin LQFP (0.5mm pitch)
AKD4617	Evaluation Board for AK4617	

■ Pin Layout



■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	IN1/IN1P, IN1N, IN2/IN2P, IN2N	Open
	LOUT1-6, ROUT1-6	Open
Digital	SDTI1-6	Connect to VSS1
	SDTO	Open

5. Pin Configurations and Functions

No.	Pin Name	I/O	Function
1	SDTI1	I	Audio Serial Data Input 1 Pin
2	LRCK	I/O	Input Channel Clock Pin
3	MCLK	I	External Master Clock Input Pin
4	BICK	I/O	Audio Serial Data Clock Pin
5	TST1	I	This pin must be connected to ground.
6	REGO	O	Regulator Output Pin This pin should be connected to ground with 1.0uF.
7	VSS1	-	Ground Pin, 0V
8	TVDD	-	Digital Power Supply Pin, 3.0V~3.6V
9	SDTO	O	Audio Serial Data Output Pin
10	TST2	O	This pin must be open.
11	SMUTEN	I	All Analog Outputs Soft Mute Pin L: Mute H: Normal Operation
12	PDN	I	Power-Down & Reset Pin When "L", the AK4617 is powered-down and the control registers are reset to default state.
13	IN1N	I	(MDIE1 bit = "1") Differential Analog Negative input 1 pin
14	IN1	I	(MDIE1 bit = "0") Single-ended Analog Input 1 pin
	IN1P	I	(MDIE1 bit = "1") Differential Analog Positive input 1 pin
15	IN2N	I	(MDIE2 bit = "1") Differential Analog Negative input 2 pin
16	IN2	I	(MDIE2 bit = "0") Single-ended Analog Input 2 pin
	IN2P	I	(MDIE2 bit = "1") Differential Analog Positive input 2 pin
17	NC	-	This pin must be open.
18	AVDD1	-	Analog Power Supply Pin, 3.0V~3.6V
19	VSS2	-	Ground Pin, 0V
20	VCOM	O	Common Voltage Output Pin, AVDD1x1/2 Large external capacitor around 1μF is used to reduce power-supply noise.
21	NC	-	This pin must be open.
22	NC	-	This pin must be open.
23	NC	-	This pin must be open.
24	NC	-	This pin must be open.
25	ROUT6	O	Rch Analog Output 6 Pin
26	LOUT6	O	Lch Analog Output 6 Pin
27	ROUT5	O	Rch Analog Output 5 Pin
28	LOUT5	O	Lch Analog Output 5 Pin
29	ROUT4	O	Rch Analog Output 4 Pin
30	LOUT4	O	Lch Analog Output 4 Pin
31	ROUT3	O	Rch Analog Output 3 Pin
32	LOUT3	O	Lch Analog Output 3 Pin
33	ROUT2	O	Rch Analog Output 2 Pin
34	LOUT2	O	Lch Analog Output 2 Pin
35	ROUT1	O	Rch Analog Output 1 Pin

36	LOUT1	O	Lch Analog Output 1 Pin
37	AVDD2	-	Analog Power Supply Pin, 3.0V~3.6V
38	VSS3	-	Ground Pin, 0V
39	SPI	I	Control Mode Select Pin "L": I^2C Bus or Parallel control mode, "H": 3-wire serial control mode
40	CAD1	I	(SPI pin = "H") (SPI pin = "L", PS pin= "L") Chip Address Pin in serial control mode
	TDM0	I	(SPI pin = "L", PS pin= "H") TDM I/F Format Mode 0 Pin in parallel control mode "L": Normal mode, "H": TDM mode
41	CSN	I	(SPI pin = "H") Chip Select Pin in 3-wire serial control mode
	PS	I	(SPI pin = "L") Control Mode Select Pin "L": I^2C Bus serial control mode, "H": Parallel control mode
42	CDTI	I	(SPI pin = "H") Control Data Input Pin in 3-wire serial control mode
	SDA	I/O	(SPI pin = "L", PS pin= "L") Control Data Input Pin in I^2C Bus Serial control mode
	DIF	I	(SPI pin = "L", PS pin= "H") Audio Data Interface Format Pin in parallel control mode "L":24bit, Left justified, "H": 24bit, I^2S
43	CCLK	I	(SPI pin = "H") Control Data Clock Pin in 3-wire serial control mode
	SCL	I	(SPI pin = "L", PS pin= "L") Control Data Clock Pin in I^2C Bus serial control mode
	MS	I	(SPI pin = "L", PS pin= "H") Master Mode Select Pin "L": Slave Mode "H": Master Mode
44	SDTI6	I	(TDM1-0 bit = "00") Audio Serial Data Input 6 Pin/
	TDMI	I	(TDM1-0 bit = "01" or "10") TDM Data Input Pin
45	SDTI5	I	Audio Serial Data Input 5 Pin
46	SDTI4	I	Audio Serial Data Input 4 Pin
47	SDTI3	I	Audio Serial Data Input 3 Pin
48	SDTI2	I	Audio Serial Data Input 2 Pin

Note 1. All digital input pins must not be allowed to float.

6. Absolute Maximum Ratings

(VSS1 ~ 3 = 0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies	Analog1	AVDD1,	-0.3	6.0	V
	Analog2	AVDD2	-0.3	6.0	V
	Digital1	TVDD	-0.3	6.0	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD1+0.3	V
Digital Input Voltage (SDTI1-6, SPI, CSN/PS, CCLK/ SCL/MS, CDTI/SDA/DIF, CAD1/TDM0, PDN pins)		VIND	-0.3	TVDD+0.3	V
Ambient Temperature (power applied)(Note 3)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground. VSS1 ~ 3 must be connected to the same analog ground plane.
Note 3. In case that PCB wiring density is 100%.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 ~ 3 = 0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 4)	Analog	AVDD1, AVDD2	3.0	3.3	3.6	V
	Digital	TVDD	3.0	3.3	3.6	V
	Difference	AVDD1, AVDD2 – TVDD	-0.1	0	+0.1	V

Note 4. The power up sequence between AVDD1, AVDD2 and TVDD is not critical. Each power supplies should be powered up during the PDN pin = "L". The PDN pin should be "H" after all power supplies are powered up. All power supplies should be powered on, only a part of these power supplies cannot be powered off. (Power off means power supplies equal to ground or power supplies are floating.) Do not turn off only the AK4617 under the condition that a surrounding device is powered on and the I^2C bus is in use. AVDD1 and AVDD2 must be connected with the same power supply.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Analog Characteristics

(Ta=25ºC; AVDD1, AVDD2=TVDD=3.3V, VSS1 ~ 3 =0V, BICK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~20kHz @fs=48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz; Unless otherwise specified.)

Parameter			min	typ	max	Unit
ADC Analog Input Characteristics(Single-ended inputs)						
Resolution					24	bit
S/(N+D)	(-1dBFS)		77	87		dB
DR (-60dBFS with A-weighted)			87	97		dB
S/N	(A-weighted)		87	97		dB
Interchannel Isolation				110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Input Voltage	Single-ended (AIN=0.81x AVDD1)		2.40	2.67	2.94	Vpp
Power Supply Rejection		(Note 5)		60		dB
DAC Analog Output Characteristics (Single-ended outputs)						
Resolution					24	bit
S/(N+D)	(0dBFS)	fs=48kHz BW=20kHz	85	95		dB
		fs=96kHz BW=40kHz		93		
		fs=192kHz BW=40kHz		93		
DR	(-60dBFS with A-weighted)		100	106		dB
S/N	(A-weighted)		100	106		dB
Interchannel Isolation				100		dB
Interchannel Gain Mismatch (Note 6)				0	0.7	dB
Gain Drift				20	-	ppm/°C
Output Voltage	AOUT=0.76 x AVDD2		2.25	2.51	2.77	Vpp
Load Resistance	(AC Load)		5			kΩ
Load Capacitance					30	pF
Power Supply Rejection (Note 5)				60		dB

Note 5. PSR is applied to AVDD1, AVDD2 and TVDD with 1kHz, 50mVpp.
Note 6. Channel gain mismatch between all output channels (LOUT1-6, ROUT1-6).

Parameter		min	typ	max	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
AVDD1+AVDD2	fs=48kHz		45	59	mA
AVDD1+AVDD2	fs=96kHz, 192kHz		40		mA
TVDD	fs=48kHz		6	8	mA
TVDD	fs=96kHz		7		mA
TVDD	fs=192kHz		9		mA
Power-down mode (PDN pin = "L") (Note 7)					
AVDD1+AVDD2+TVDD			10	200	μA

Note 7. In the power-down mode, all digital input pins including clock pins are held VSS1.

9. ADC Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF(SD_AD bit="0")						
Passband (Note 8)	±0.16dB	PB	0	-	18.8	kHz
	–0.28dB		-	20.0	-	kHz
	–3.0dB		-	22.8	-	kHz
Stopband(Note 8)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	71	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	15.5	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER(SD_AD bit="1")						
Passband (Note 8)	±0.16dB	PB	0	-	18.8	kHz
	–0.28dB		-	20.0	-	kHz
	–3.0dB		-	22.8	-	kHz
Stopband (Note 8)		SB	28.4		-	-
Stopband Attenuation		SA	72		-	-
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	2.4	1/fs
Group Delay (Note 10)		GD	-	5.5	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3.0dB	FR	-	3.7	-	Hz
	–0.5dB		-	10.9	-	Hz
	–0.1dB		-	24.0	-	Hz

10. DAC Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF): SHARP ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB –6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	21.4	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR	-	-0.1	-	dB
DAC Digital Filter (LPF): SLOW ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB –6.0dB	PB	0 -	 22.5	9.8 -	kHz kHz
Stopband		SB	40.1			kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		9.0		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR		-4.0		dB
DAC Digital Filter (LPF): SHORT DELAY SHARP ROLL-OFF (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB –6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	8.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR		-0.1		dB
DAC Digital Filter (LPF): SHORT DELAY SLOW ROLL-OFF FILTER (DEM=OFF; SD_DA bit="1"; SLOW bit="1")						
Passband (Note 9)	±0.06dB –6.0dB	PB	0 -	- 22.5	9.8 -	kHz kHz
Stopband		SB	40.1	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0~20.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	7.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR	-	-4.0	-	dB

11. DAC Filter Characteristics (fs=96kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF): SHARP ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 48.0	43.6 -	kHz kHz
Stopband		SB	52.4	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	21.4	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR	-	-0.3	-	dB
DAC Digital Filter (LPF): SLOW ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	 45.0	19.6 -	kHz kHz
Stopband		SB	80.2			kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		9.0		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR		-4.2		dB
DAC Digital Filter (LPF): SHORT DELAY SHARP ROLL-OFF (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 48.0	43.6 -	kHz kHz
Stopband		SB	52.4	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	8.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR		-0.3		dB
DAC Digital Filter (LPF): SHORT DELAY SLOW ROLL-OFF FILTER (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	- 45.0	19.6 -	kHz kHz
Stopband		SB	80.2	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	7.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR	-	-4.2	-	dB

12. DAC Filter Characteristics (fs=192kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF): SHARP ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 96.0	87.2 -	kHz kHz
Stopband		SB	104.8	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	21.4	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR	-	-1.0	-	dB
DAC Digital Filter (LPF): SLOW ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	 90.0	39.2 -	kHz kHz
Stopband		SB	160.4			kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		9.0		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR		-5.0		dB
DAC Digital Filter (LPF): SHORT DELAY SHARP ROLL-OFF (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 96.0	87.2 -	kHz kHz
Stopband		SB	104.8	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	8.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR		-1.0		dB
DAC Digital Filter (LPF): SHORT DELAY SLOW ROLL-OFF FILTER (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	- 90.0	39.2 -	kHz kHz
Stopband		SB	160.4	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	7.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR	-	-5.0	-	dB

Note 8. The passband and stopband frequencies scale with fs (sampling frequency). For example, ADC: Passband (±0.1dB) = 0.375 x fs, DAC: Passband (±0.06dB) = 0.454 x fs.

Note 9. The passband and stopband frequencies scale with fs (sampling frequency). For example, DAC: Passband (±0.06dB) = 0.204 x fs.

Note 10. The calculated delay time is resulting from digital filtering. For the ADC, this time is from the input of an analog signal to the setting of 24bit data for both channels to the ADC output register. For the DAC, this time is from setting the 24 bit data both channels at the input register to the output of an analog signal.
Note 11. The reference frequency is 1kHz.
Note 12. It is the gain amplitude in passband.

13. DC Characteristics

(Ta=-40~+105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SPI, CSN/PS, CCLK/SCL/MS, CDTI/SDA/DIF, CAD1/TDM0, PDN pins)	VIH	70% TVDD	-	-	V
Low-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SPI, CSN/PS, CCLK/SCL/MS, CDTI/SDA/DIF, CAD1/TDM0, PDN pins)	VIL	-	-	30% TVDD	V
High-Level Output Voltage (LRCK, BICK, SDTO pins: Iout=-100µA)	VOH	TVDD-0.5	-	-	V
Low-Level Output Voltage (LRCK, BICK, SDTO pins: Iout= 100µA)	VOL		-	0.5	V
(SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	µA

14. Switching Characteristics

(Ta=-40~+105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
External Clock					
256fsn:	fCLK	2.048		12.288	MHz
Pulse Width Low	tCLKL	32			ns
Pulse Width High	tCLKH	32			ns
384fsn:	fCLK	3.072		18.432	MHz
Pulse Width Low	tCLKL	22			ns
Pulse Width High	tCLKH	22			ns
512fsn:	fCLK	4.096		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
LRCK Timing (Slave mode)					
Stereo mode (Figure 2)					
(TDM1-0 bit = "00")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	45		55	%
TDM512 mode (Figure 3),(Note 13)					
(TDM1-0 bit = "01")					
LRCK frequency	fsn	8		48	kHz
"H" time	tLRH	1/512fs			ns
"L" time	tLRL	1/512fs			ns
TDM256 mode (Figure 3),(Note 14)					
(TDM1-0 bit = "10")					
LRCK frequency	fsn	8		48	kHz
	fsd	64		96	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 mode (Figure 3),(Note 15)					
(TDM1-0 bit = "11")					
LRCK frequency	fsq	128		192	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns

LRCK Timing (Master Mode)					
Stereo mode (Figure 4) **(TDM1-0 bit = "00")**					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	-	50	-	%
TDM512 mode (Figure 5),(Note 13) **(TDM1-0 bit = "01")**					
LRCK frequency	fsn	8		48	kHz
"H" time (Note 16)	tLRH		1/16fs		ns
TDM256 mode (Figure 5),(Note 14) **(TDM1-0 bit = "10")**					
LRCK frequency	fsn	8		48	kHz
	fsd	64		96	kHz
"H" time (Note 16)	tLRH		1/8fs		ns
TDM128 mode (Figure 5),(Note 15) **(TDM1-0 bit = "11")**					
LRCK frequency	fsq	128		192	kHz
"H" time (Note 16)	tLRH		1/4fs		ns

Note 13. Please use for Normal Speed mode. Master clock should be input the 512fs in Master mode.
Note 14. Please use for Normal Speed mode, Double Speed mode. Master clock should be input the 256fs or 512fs in Master mode.
Note 15. Please use for Quad Speed mode. Master clock should be input the 128fs in Master mode.
Note 16. If the format is I^2S, it is "L" time.

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Slave mode)					
Stereo mode (TDM1-0 bit = "00") for Normal Speed mode (Figure 2, Figure 6)					
BICK Period	tBCK	324			ns
BICK Pulse Width Low	tBCKL	130			ns
Pulse Width High	tBCKH	130			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	20			ns
LRCK to SDTO(MSB) (Except I^{2}S mode)	tLRS			80	ns
BICK "↓" to SDTO	tBSD			80	ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns
Stereo mode (TDM1-0 bit = "00") for Double and Quad Speed mode (Figure 2, Figure 6)					
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	33			ns
Pulse Width High	tBCKH	33			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	23			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	23			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM512 mode (TDM1-0 bit = "01") (Note 13) (Figure 3, Figure 7)					ns
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM256 mode (TDM1-0 bit = "10") (Note 14) (Figure 3, Figure 7)					ns
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM128 mode (TDM1-0 bit = "11") (Note 15) (Figure 3, Figure 7)					
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	10			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Master mode)					
Stereo mode (TDM1-0 bit = "00") for Normal Speed mode (Figure 4, Figure 8)					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–80	-	80	ns
BICK "↓" to SDTO	tBSD	–80	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Stereo mode (TDM1-0 bit = "00") for Double and Quad Speed mode (Figure 4, Figure 8)					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty (Table 17)	dBCK	-	50	-	%
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM512 mode (TDM1-0 bit = "01") (Note 13) (Figure 5, Figure 9)					
BICK Frequency	fBCK	-	512fs	-	Hz
BICK Duty (Table 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	-10		10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI Hold Time	tSDH	5	-	-	ns
SDTI Setup Time	tSDS	6	-	-	ns
TDM256 mode (TDM1-0 bit = "10") (Note 14) (Figure 5, Figure 9)					
BICK Frequency	fBCK	-	256fs	-	Hz
BICK Duty (Table 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	--	ns
SDTI Hold Time	tSDH	5	-	-	ns
SDTI Setup Time	tSDS	6	-		ns
TDM128 mode (TDM1-0 bit = "11") (Note 15) (Figure 5, Figure 9)					
BICK Frequency	fBCK	-	128fs	-	Hz
BICK Duty (Table 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns

Note 17. BICK rising edge must not occur at the same time as LRCK edge.
Note 18. In the case that the duty of MCLK is 50%.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 19)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 20)	tPD	150			ns
PDN "↑" to SDTO valid (Note 21)	tPDV		32768/MCLK +1059/fs		s

Note 19. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 20. The AK4617 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 150ns for a certain reset. The AK4617 is not reset by the "L" pulse less than 30ns.

Note 21. These cycles are the numbers of MCLK and LRCK rising from the PDN pin rising.

Note 22. I^2C is a trademark of NXP B.V.

■ Timing Diagram

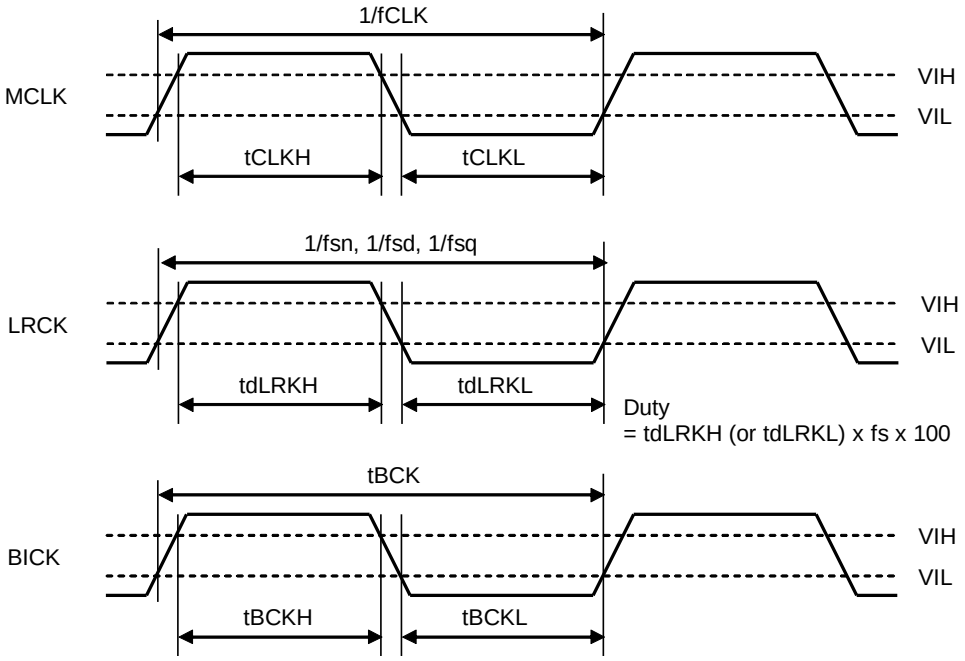


Figure 2. Clock Timing (TDM1-0 bit = "00" & Slave mode)

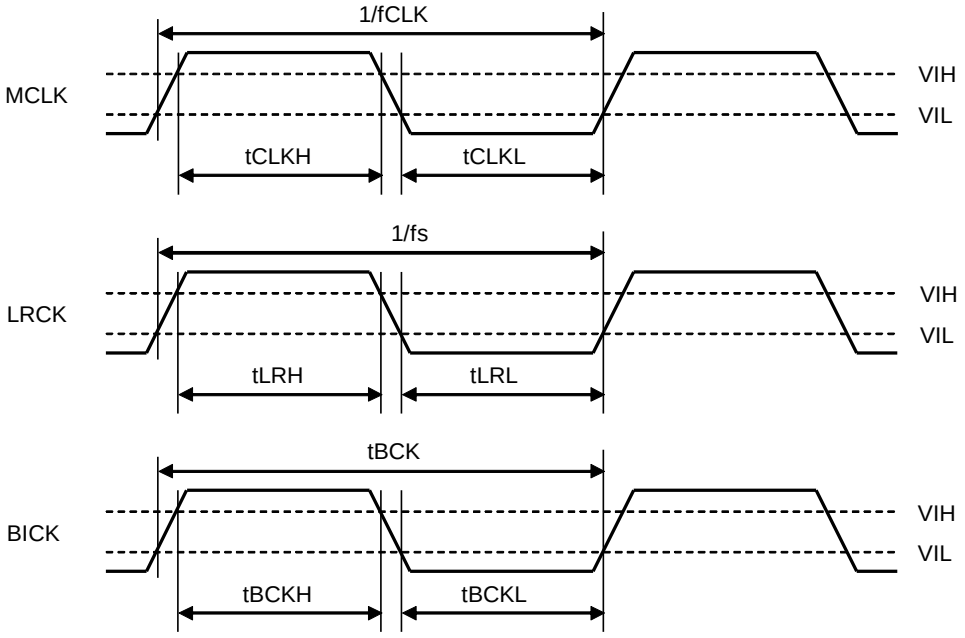


Figure 3. Clock Timing (Except TDM1-0 bit = "00" & Slave mode)

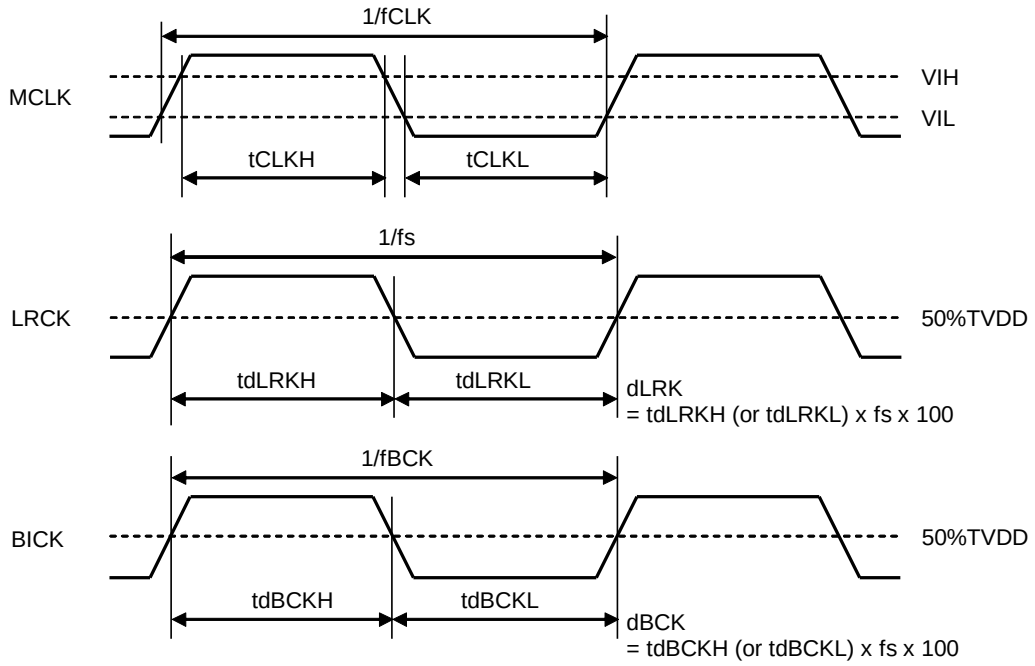


Figure 4. Clock Timing (TDM1-0 bit = "00" & Master mode)

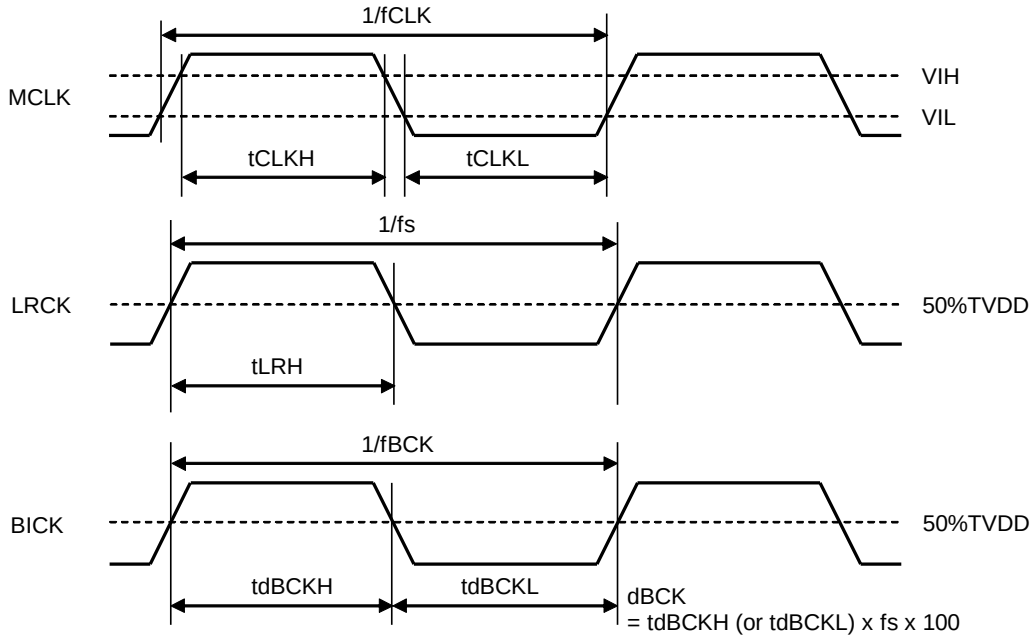


Figure 5. Clock Timing (Except TDM1-0 bit = "00" & Master mode)

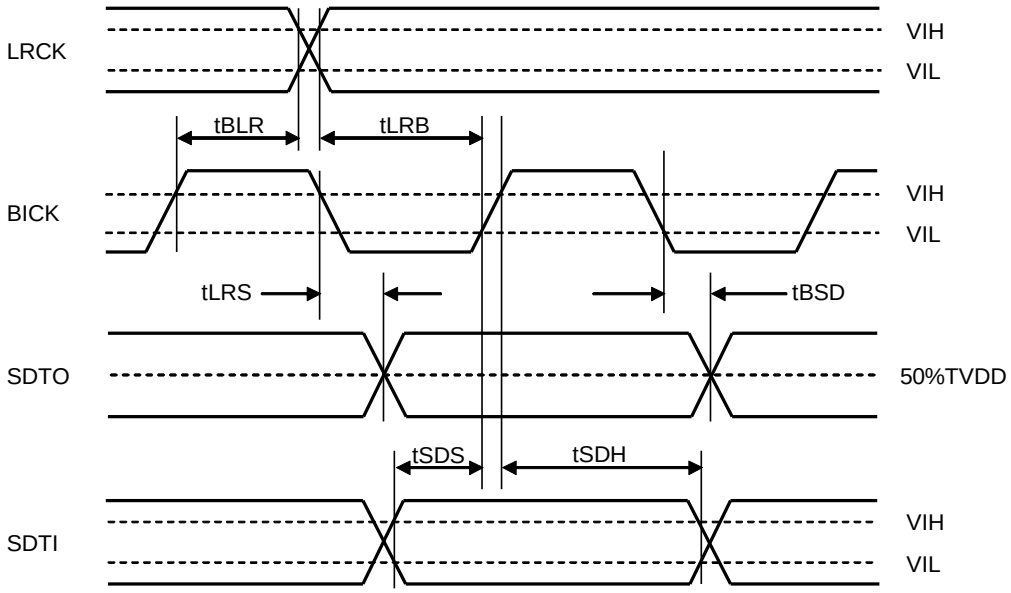


Figure 6. Audio Interface Timing (TDM1-0 bit = "00" & Slave mode)

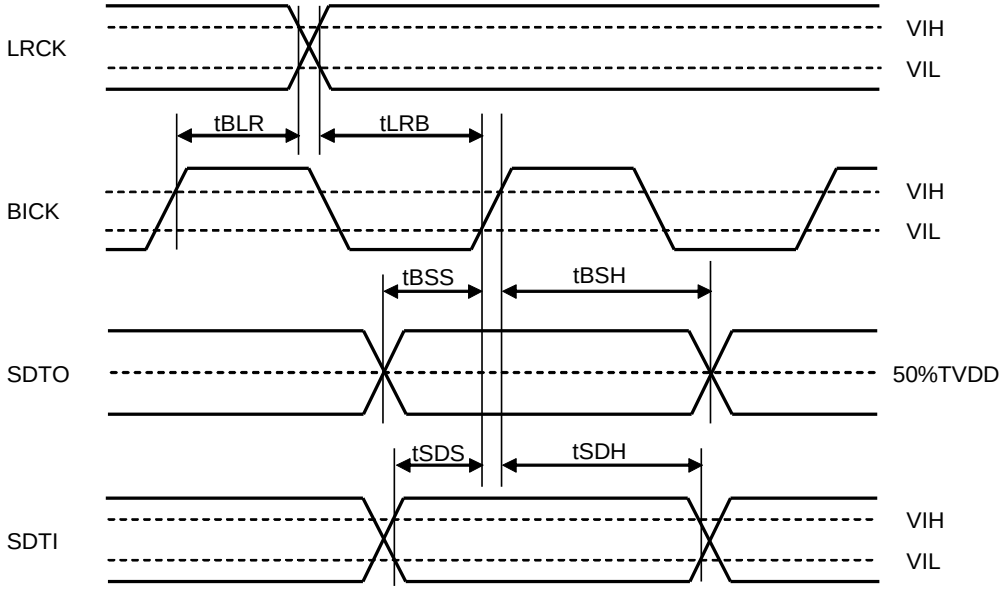


Figure 7. Audio Interface Timing (Except TDM1-0 bit = "00" & Slave mode)

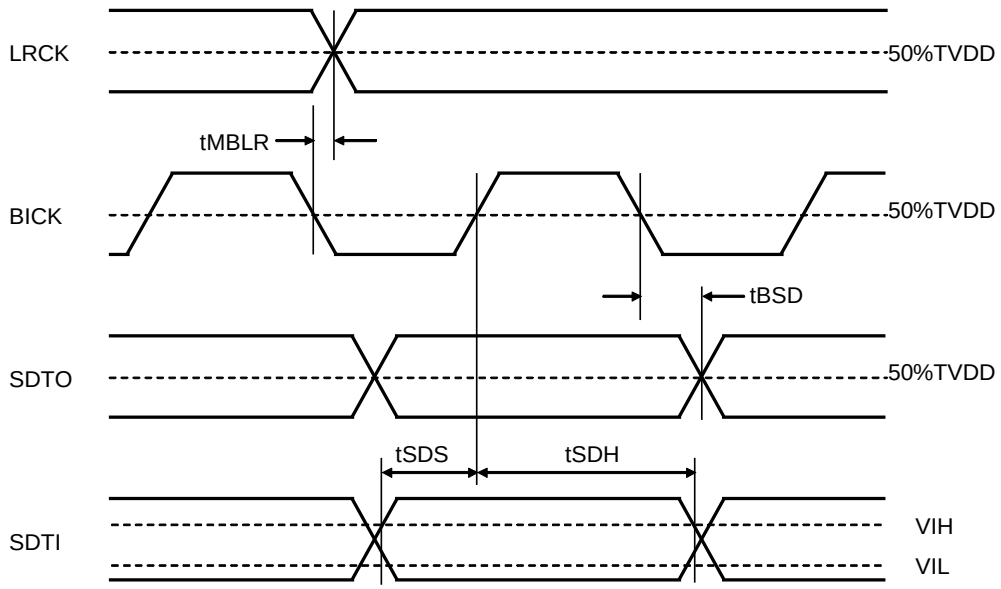


Figure 8. Audio Interface Timing (TDM1-0 bit = "00" & Master mode)

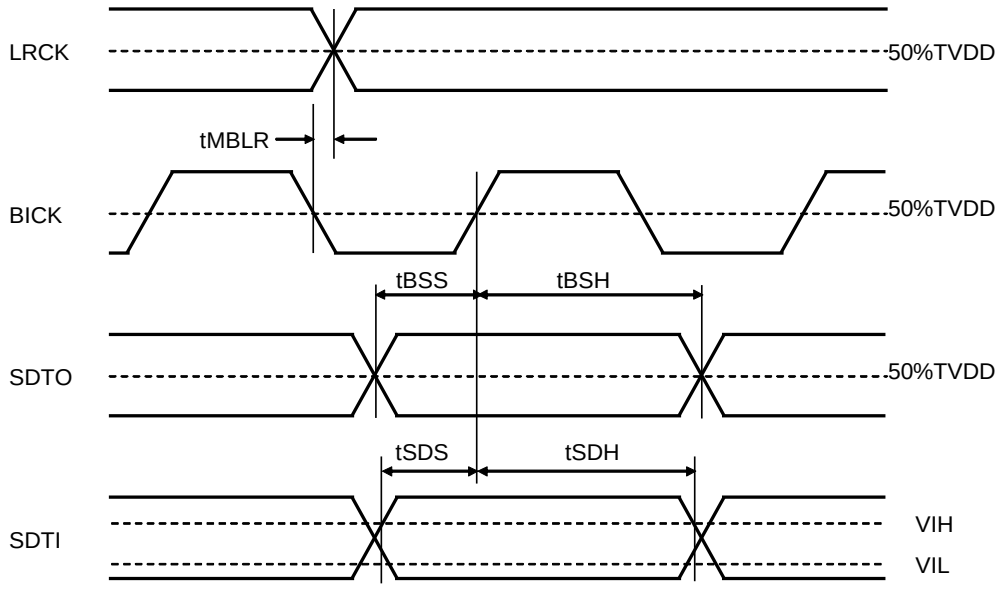


Figure 9. Audio Interface Timing (Except TDM1-0 bit = "00" & Master mode)

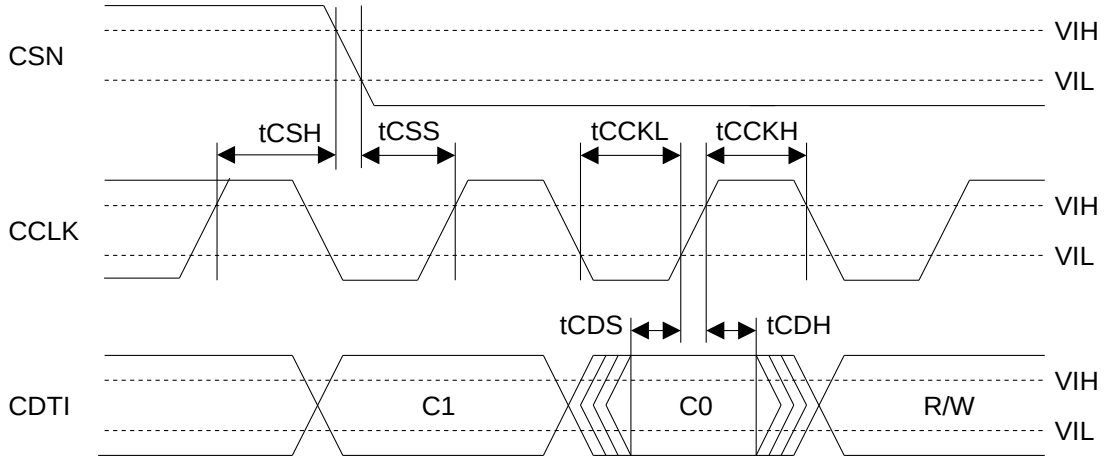


Figure 10. WRITE Command Input Timing (3-wire Serial mode)

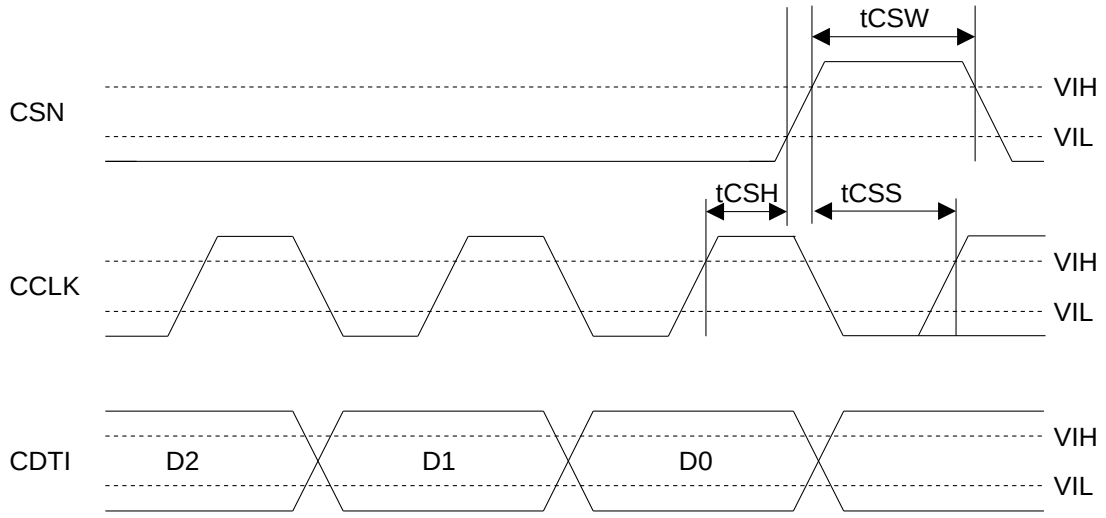


Figure 11. WRITE Data Input Timing (3-wire Serial mode)

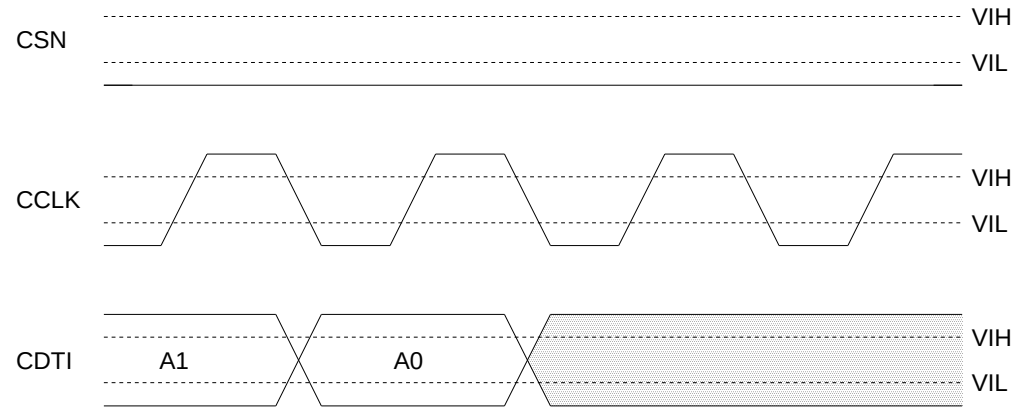


Figure 12. Read Data Output Timing1(3-wire Serial mode)

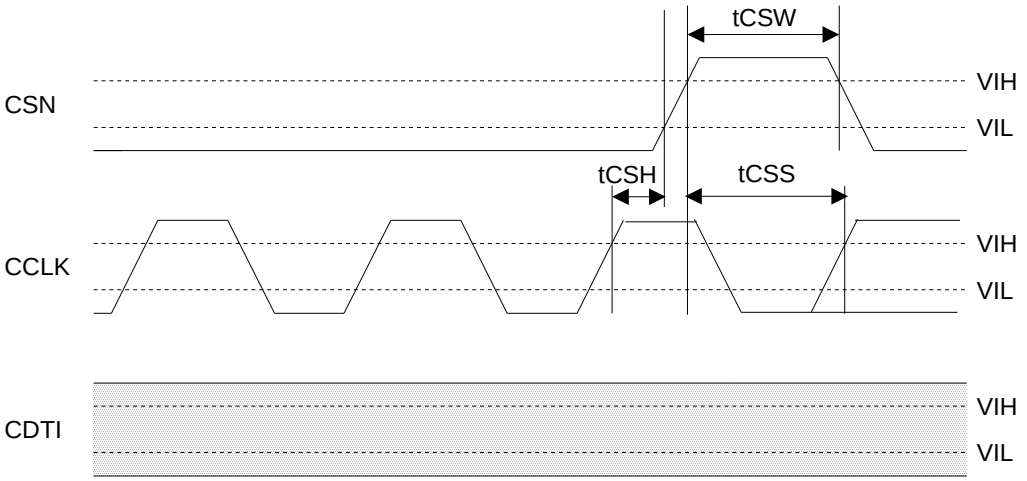


Figure 13. Read Data Output Timing2(3-wire Serial mode)

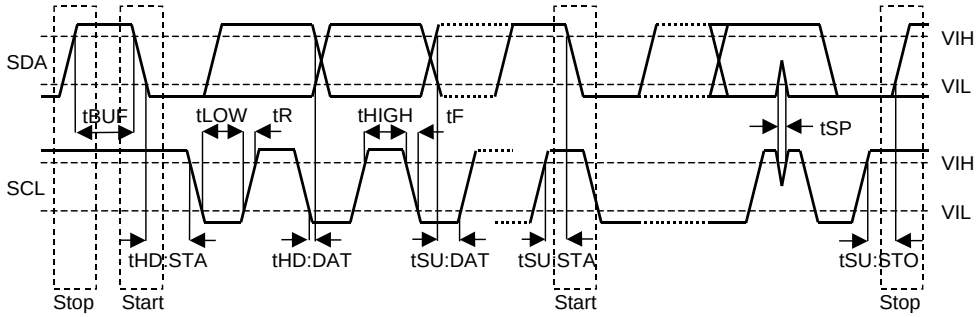


Figure 14. I^2C Bus mode Timing

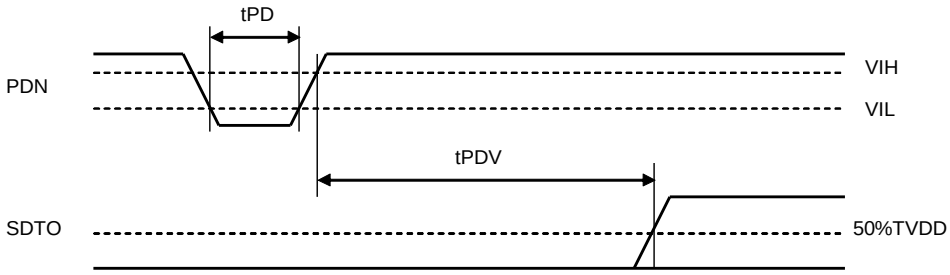


Figure 15. Power-down & Reset Timing

15. Functional Descriptions

■ System Clock

The external clocks which are required to operate the AK4617 in slave mode are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK but the phase is not critical. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit= "0": Default), the sampling speed is set by DFS0, DFS1 (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 3, Table 4, Table 5). In Auto Setting Mode (ACKS bit= "1"), as MCLK frequency is detected automatically (Table 6) and the internal master clock attains the appropriate frequency (Table 7), so it is not necessary to set DFS.

In master mode, only MCLK is required. Master Clock Input Frequency should be set with the CKS1-0 bit, and the sampling speed should be set by the DFS1-0 bit. The frequencies and the duties of the clocks (LRCK, BICK) are not stabile immediately after setting CKS1-0 bit and DFS1-0 bit up.

After exiting reset at power-up in slave mode, the AK4617 is in power-down mode until MCLK and LRCK are input.

If the clock is stopped, click noise occurs when restarting the clock. Mute the digital output externally.

Note: ADC is automatically powered-down in Double Speed Mode and Quad Speed Mode.

DFS1	DFS0	Sampling Speed Mode (fs)	
0	0	Normal Speed Mode	8kHz~48kHz
0	1	Double Speed Mode	64kHz~96kHz
1	0	Quad Speed Mode	128kHz~192kHz
1	1	N/A	-

(default)

(N/A: Not available)

Table 1. Sampling Speed (Manual Setting Mode)

CKS1	CKS0	Normal Speed Mode	Double Speed Mode	Quad Speed Mode	
0	0	256fs	256fs	128fs	
0	1	384fs	256fs	128fs	
1	0	512fs	256fs	128fs	(default)
1	1	512fs	256fs	128fs	

Table 2. Master Clock Input Frequency Select (Master Mode)

Note: In Normal Speed Mode, TDM mode (TDM1-0 bit ="01) can be used when CKS1 bit = "1".

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
32.0kHz	8.1920	12.2880	16.3840	2.0480
44.1kHz	11.2896	16.9344	22.5792	2.8224
48.0kHz	12.2880	18.4320	24.5760	3.0720

Table 3. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)	BICK (MHz)
fs	256fs	64fs
88.2kHz	22.5792	5.6448
96.0kHz	24.5760	6.1440

Table 4. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)	BICK (MHz)
fs	128fs	64fs
176.4kHz	22.5792	11.2896
192.0kHz	24.5760	12.2880

Table 5. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK	Sampling Speed Mode
512fs	Normal Speed Mode
256fs	Double Speed Mode
128fs	Quad Speed Mode

Table 6. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)			Sampling Speed Mode
fs	128fs	256fs	512fs	
32.0kHz	-	-	16.3840	Normal Speed Mode
44.1kHz	-	-	22.5792	
48.0kHz	-	-	24.5760	
88.2kHz	-	22.5792	-	Double Speed Mode
96.0kHz	-	24.5760	-	
176.4kHz	22.5792	-	-	Quad Speed Mode
192.0kHz	24.5760	-	-	

Table 7. System Clock Example (Auto Setting Mode)

■ De-emphasis Filter

The AK4617 has a digital de-emphasis filter (tc=50/15μs) by an IIR filter. The de-emphasis filter supports only Normal Speed Mode. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis of each DAC can be set individually by registers, DAC1(SDTI1), DAC2(SDTI2), DAC3(SDTI3), DAC4(SDTI4), DAC5(SDTI5), DAC6(SDTI6).

Mode	Sampling Speed Mode	DEM11 (DEM61-21)	DEM10 (DEM60-20)	DEM	
0	Normal Speed Mode	0	0	44.1kHz	
1	Normal Speed Mode	0	1	OFF	(default)
2	Normal Speed Mode	1	0	48kHz	
3	Normal Speed Mode	1	1	32kHz	

Table 8. De-emphasis control

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 3.7Hz at fs=48kHz and scales with the sampling rate (fs).

■ Master Mode and Slave Mode

Master Mode and Slave Mode are selected by setting the MS pin in Parallel control mode. (Master Mode= "H", Slave Mode= "L")
LRCK and BICK pins are outputs in Master Mode (MS pin= "H")
LRCK and BICK pins are inputs in Slave Mode (MS pin= "L")

In the serial control mode, BICK and LRCK pins are Hi-z before an internal power up and MS bit = "1".
In the parallel control mode, BICK and LRCK pins are Hi-z before an internal power up.
When a problem is occurred by this, pull down BICK and LRCK pins by external resistance (ex. 100kohm).

PDN	MS pin	LRCK pin	BICK pin
L	L	Input	Input
	H	Hi-z	Hi-z
H	L	Input	Input
	H	Output	Output

Table 9. LRCK and BICK pins

■ Audio Serial Interface Format

(1) Stereo Mode

When TDM1-0 bit = "00", ten modes can be selected by the DIF2-0 bit as shown in Table 10. In all modes the serial data is MSB-first, 2's compliment format. The data SDTO is clocked out on the falling edge of BICK and the SDTI1-6 is latched on the rising edge of BICK.

Mode3/4/8/9/13/14/18/19/23/24/28/29/33/34/38/39 in SDTI input formats can be used for 16-20bit data by zeroing the unused LSBs.

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO	SDTI1-6	LRCK		BICK		
										I/O		I/O	
0	0	0	0	0	0	0	24bit, Left justified (*)	16bit, Right justified	H/L	I	≥32fs 64fs≥	I	
1	0	0	0	0	0	1	24bit, Left justified	20bit, Right justified	H/L	I	≥48fs 64fs≥	I	
2	0	0	0	0	1	0	24bit, Left justified	24bit, Right justified	H/L	I	≥48fs 64fs≥	I	
3	0	0	0	0	1	1	24bit, Left justified	24bit, Left justified	H/L	I	≥48fs 64fs≥	I	
4	0	0	0	1	0	0	24bit, I^2S	24bit, I^2S	L/H	I	≥48fs 64fs≥	I	(default)
5	1	0	0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
6	1	0	0	0	0	1	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
7	1	0	0	0	1	0	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
8	1	0	0	0	1	1	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
9	1	0	0	1	0	0	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	

Table 10. Audio data formats (Stereo mode)

(*)When the BICK is less than 48fs, the output data length from SDTO is limited to the clock number of BICK in the half LRCK period.

(2) TDM Mode

The audio serial interface format is set in TDM mode by the TDM1-0 bit = "01". Five modes can be selected by the DIF2-0 bit as shown in Table 11. In all modes the serial data is MSB-first, 2's compliment format. The SDTO is clocked out on the rising edge of BICK and the SDTI1/2/3 are latched on the rising edge of BICK. In the TDM512 mode (fs = 48kHz), the serial data of all ADC (two channels) is output to the SDTO pin. And the serial data of all DAC (twelve channels) is input to the SDTI1 pin. The input data to SDTI2-6 pins are ignored and the SDTI6 pin is used as the TDMI pin. BICK should be fixed to 512fs. "H" time and "L" time of LRCK should be 1/512fs at least.
TDM256 mode can be set by TDM1-0 bit as show in Table 12. In the TDM256 mode (fs =48, 96kHz), SDTO pin = "L" @96kHz. And the serial data of DAC (eight channels; L1, R1, L2, R2, L3, R3, L4, R4) is input to the SDTI1 pin. Other four data (L5, R5, L6, R6) are input to the SDTI2 pin. The input data to SDTI3-6 pins are ignored and the SDTI6 pin is used as the TDMI pin. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be 1/256fs at least. TDM128 mode can be set by TDM1-0 bit as show in Table 13.
In TDM128 mode (fs=192kHz), SDTO pin = "L". And the serial data of DAC (four channels; L1, R1, L2, R2) is input to the SDTI1 pin and the serial data of DAC (four channels; L3, R3, L4, R4) is input to the SDTI2 pin, the serial data of DAC (four channels; L5, R5, L6, R6) is input to the SDTI3 pin. The input data to SDTI4-6 pins are ignored. BICK should be fixed to 128fs. "H" time and "L" time of LRCK should be 1/128fs at least.

Mode	M/S	TDM 1	TDM0	DIF2	DIF1	DIF0	SDTO	SDTI1	LRCK		BICK	
										I/O		I/O
10	0	0	1	0	0	0	24bit, Left justified	16bit, Right justified	↑	I	512fs	I
11	0	0	1	0	0	1	24bit, Left justified	20bit, Right justified	↑	I	512fs	I
12	0	0	1	0	1	0	24bit, Left justified	24bit, Right justified	↑	I	512fs	I
13	0	0	1	0	1	1	24bit, Left justified	24bit, Left justified	↑	I	512fs	I
14	0	0	1	1	0	0	24bit, I^2S	24bit, I^2S	↓	I	512fs	I
15	1	0	1	0	0	0	24bit, Left justified	16bit, Right justified	↑	O	512fs	O
16	1	0	1	0	0	1	24bit, Left justified	20bit, Right justified	↑	O	512fs	O
17	1	0	1	0	1	0	24bit, Left justified	24bit, Right justified	↑	O	512fs	O
18	1	0	1	0	1	1	24bit, Left justified	24bit, Left justified	↑	O	512fs	O
19	1	0	1	1	0	0	24bit, I^2S	24bit, I^2S	↓	O	512fs	O

Table 11. Audio data formats (TDM512 mode)

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO	SDTI1-2	LRCK		BICK	
										I/O		I/O
20	0	1	0	0	0	0	24bit, Left justified	16bit, Right justified	↑	I	256fs	I
21	0	1	0	0	0	1	24bit, Left justified	20bit, Right justified	↑	I	256fs	I
22	0	1	0	0	1	0	24bit, Left justified	24bit, Right justified	↑	I	256fs	I
23	0	1	0	0	1	1	24bit, Left justified	24bit, Left justified	↑	I	256fs	I
24	0	1	0	1	0	0	24bit, I^2S	24bit, I^2S	↓	I	256fs	I
25	1	1	0	0	0	0	24bit, Left justified	16bit, Right justified	↑	O	256fs	O
26	1	1	0	0	0	1	24bit, Left justified	20bit, Right justified	↑	O	256fs	O
27	1	1	0	0	1	0	24bit, Left justified	24bit, Right justified	↑	O	256fs	O
28	1	1	0	0	1	1	24bit, Left justified	24bit, Left justified	↑	O	256fs	O
29	1	1	0	1	0	0	24bit, I^2S	24bit, I^2S	↓	O	256fs	O

Table 12. Audio data formats (TDM256 mode)

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO	SDTI1-3	LRCK		BICK	
										I/O		I/O
30	0	1	1	0	0	0	L	16bit, Right justified	↑	I	128fs	I
31	0	1	1	0	0	1	L	20bit, Right justified	↑	I	128fs	I
32	0	1	1	0	1	0	L	24bit, Right justified	↑	I	128fs	I
33	0	1	1	0	1	1	L	24bit, Left justified	↑	I	128fs	I
34	0	1	1	1	0	0	L	24bit, I^2S	↓	I	128fs	I
35	1	1	1	0	0	0	L	16bit, Right justified	↑	O	128fs	O
36	1	1	1	0	0	1	L	20bit, Right justified	↑	O	128fs	O
37	1	1	1	0	1	0	L	24bit, Right justified	↑	O	128fs	O
38	1	1	1	0	1	1	L	24bit, Left justified	↑	O	128fs	O
39	1	1	1	1	0	0	L	24bit, I^2S	↓	O	128fs	O

Table 13. Audio data formats (TDM128 mode)

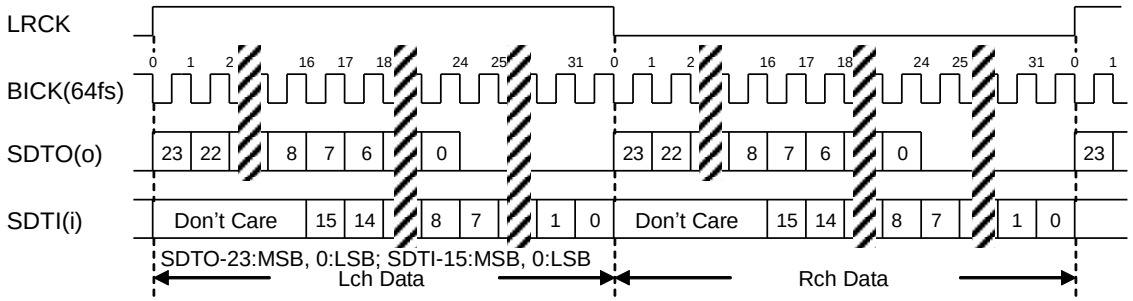


Figure 16. Mode 0/5 Timing (Stereo Mode)

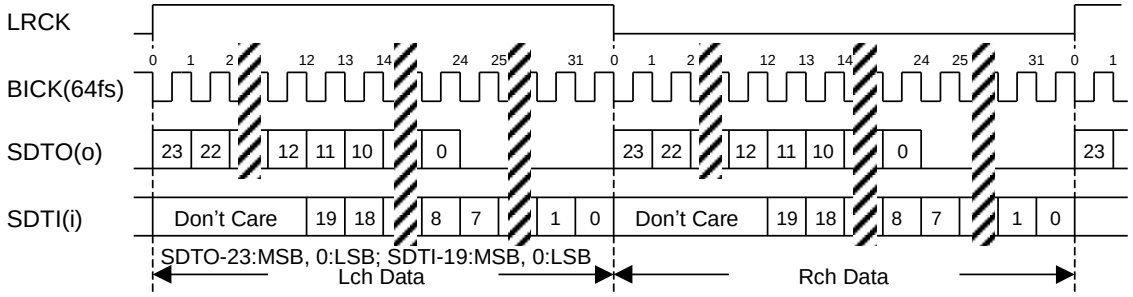


Figure 17. Mode 1/6 Timing (Stereo Mode)

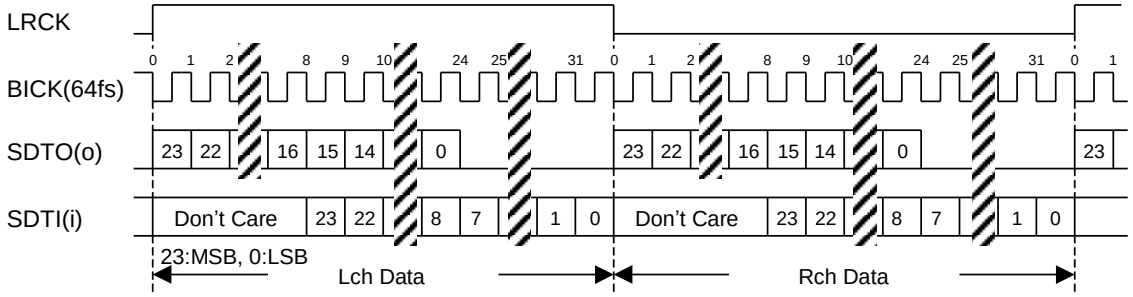


Figure 18. Mode 2/7 Timing (Stereo Mode)

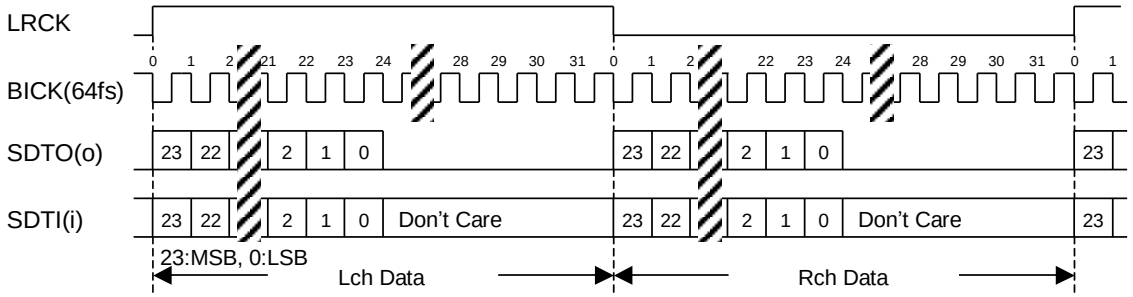


Figure 19. Mode 3/8 Timing (Stereo Mode)

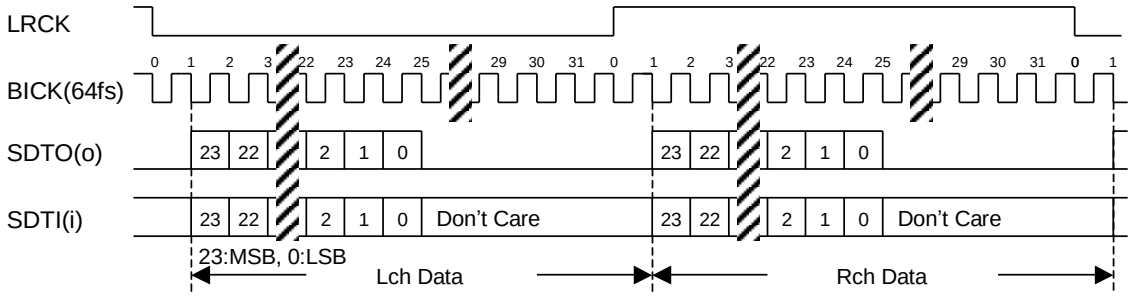
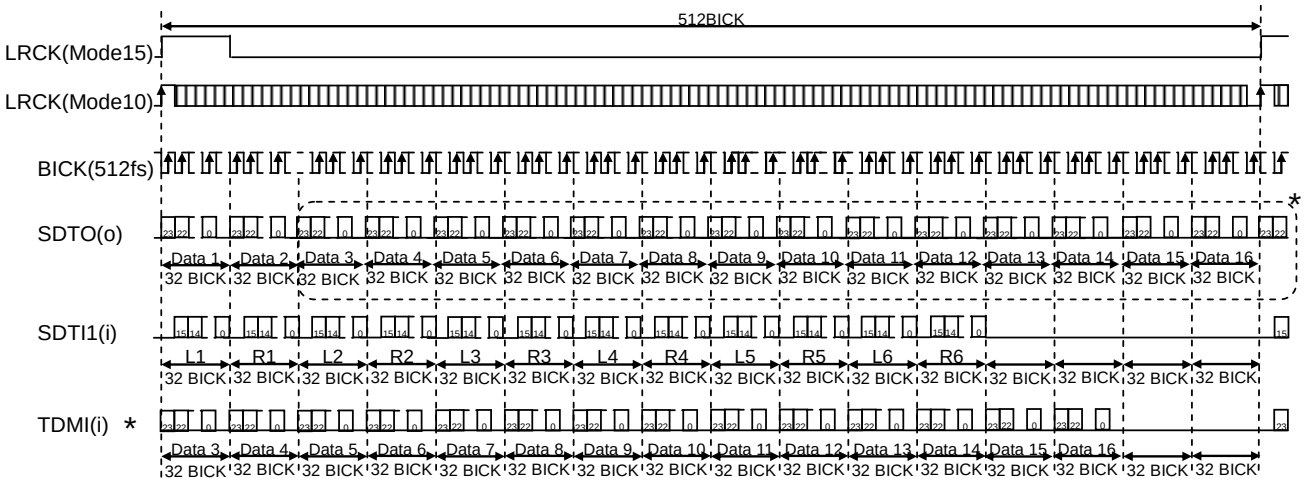
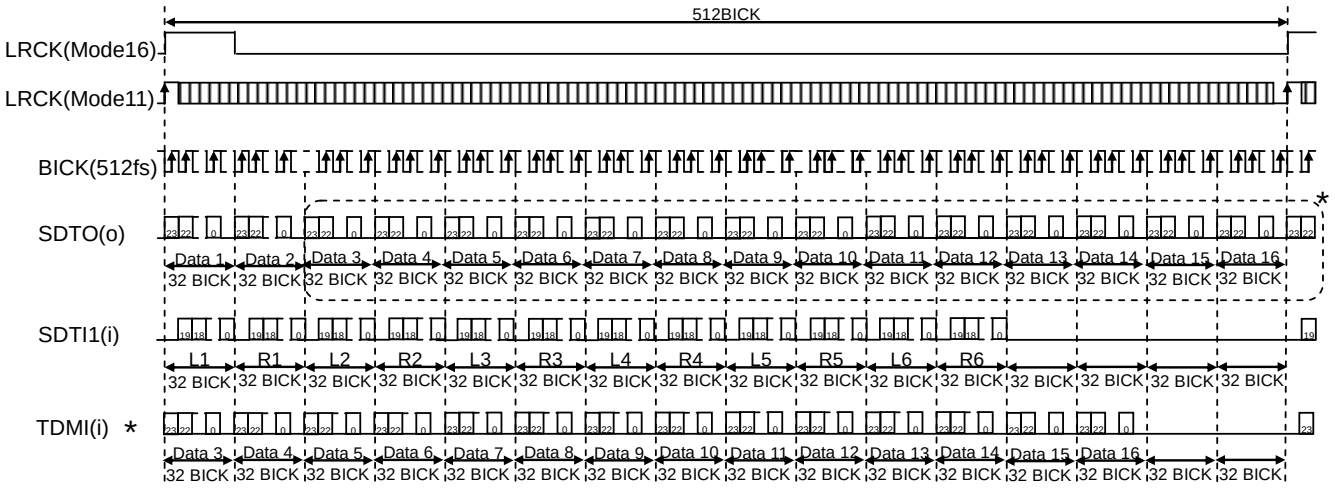


Figure 20. Mode 4/9 Timing (Stereo Mode)



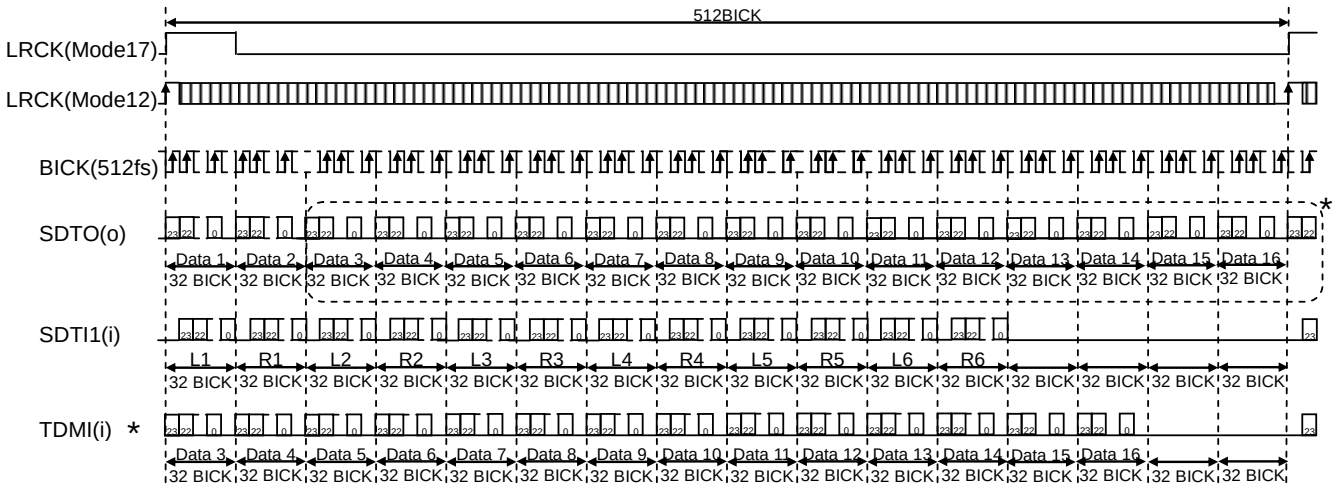
(*: Optional)

Figure 21. Mode 10/15 Timing (TDM512 Mode)



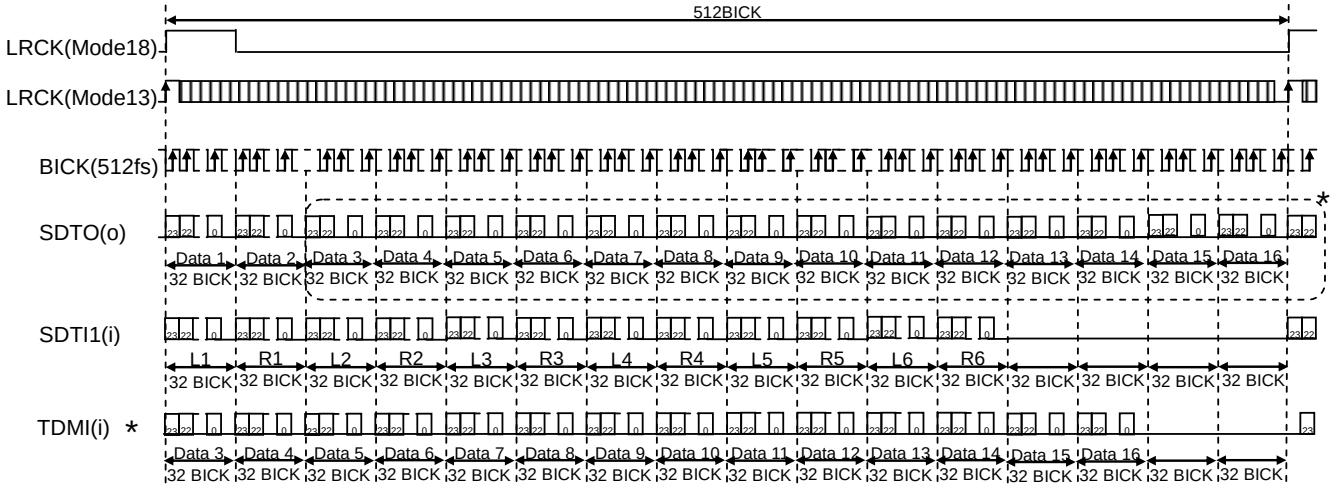
(*: Optional)

Figure 22. Mode 11/16 Timing (TDM512 Mode)



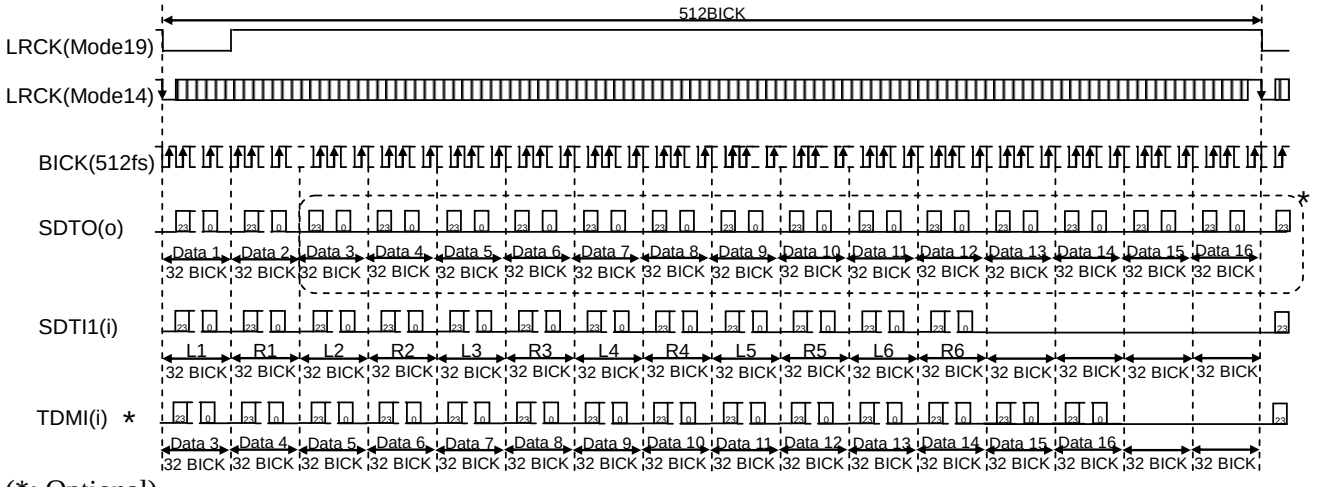
(*: Optional)

Figure 23. Mode 12/17 Timing (TDM512 Mode)



(*: Optional)

Figure 24. Mode 13/18 Timing (TDM512 Mode)



(*: Optional)

Figure 25. Mode 14/19 Timing (TDM512 Mode)

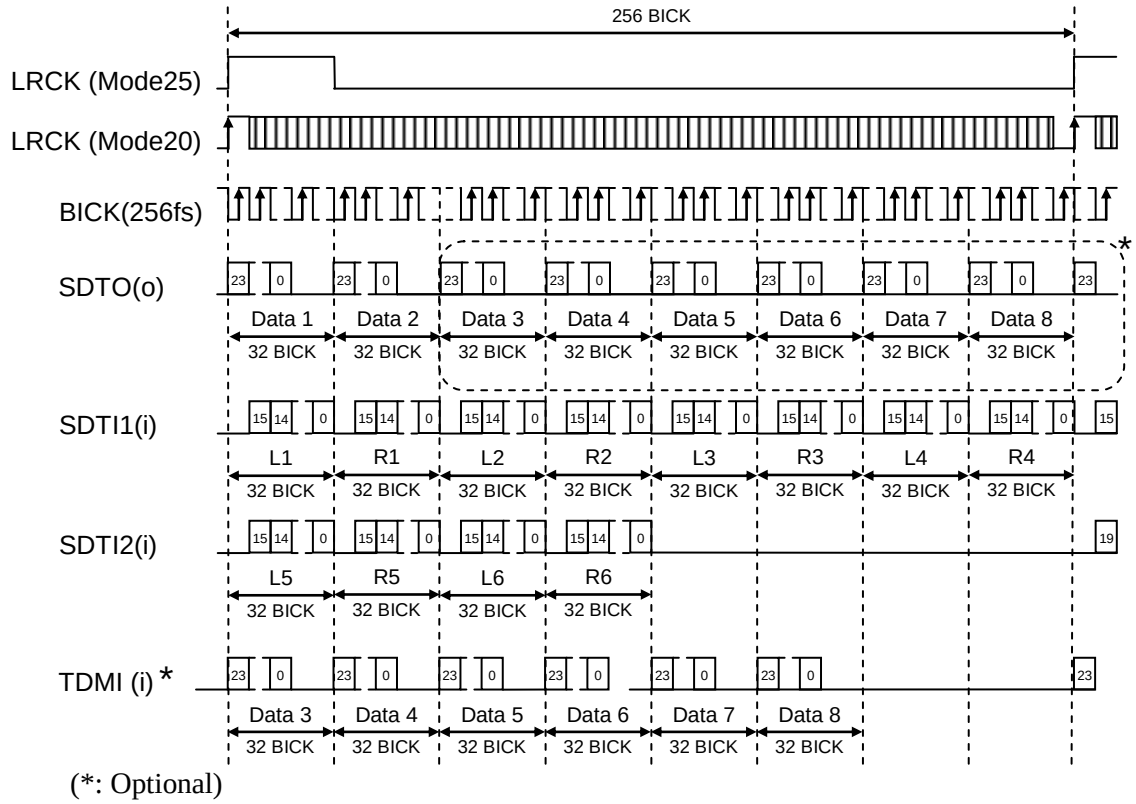


Figure 26. Mode 20/25 Timing (TDM256 Mode)

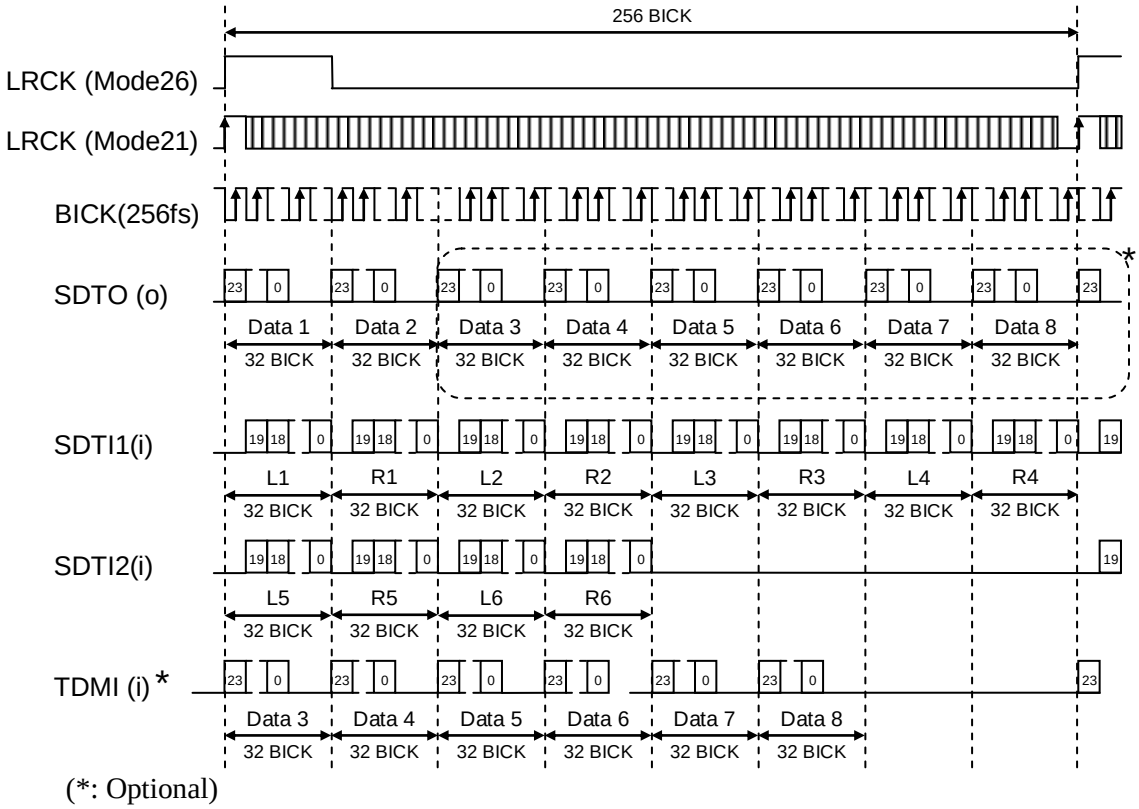
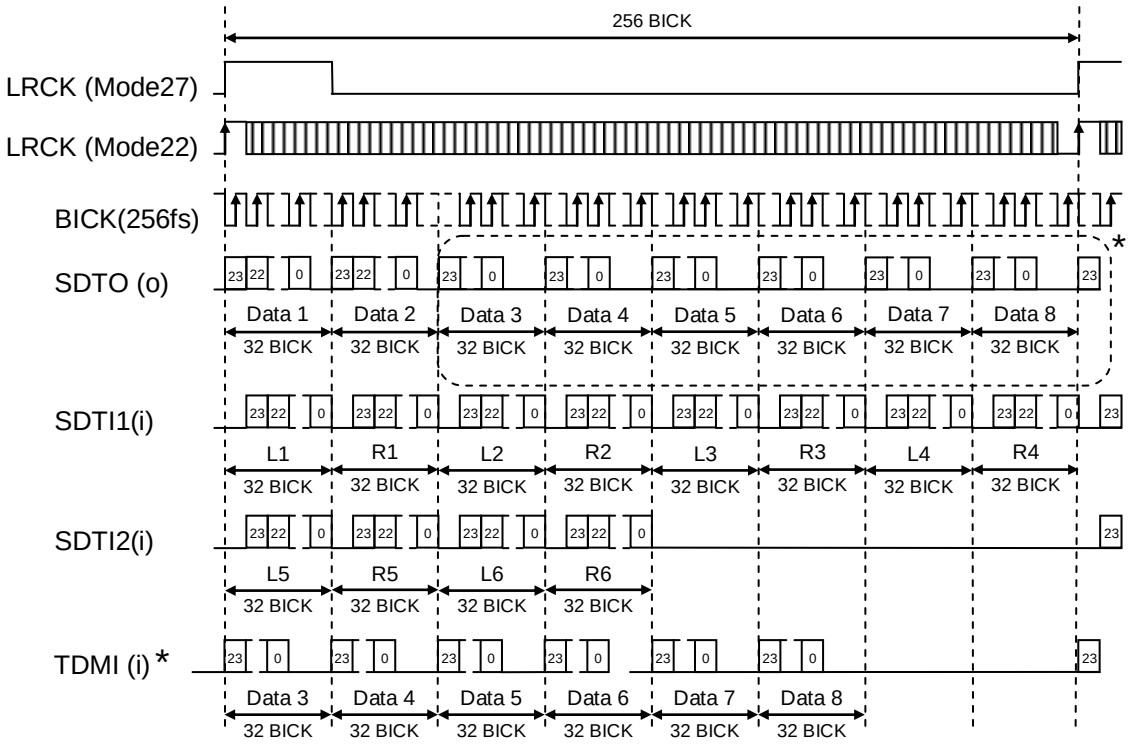
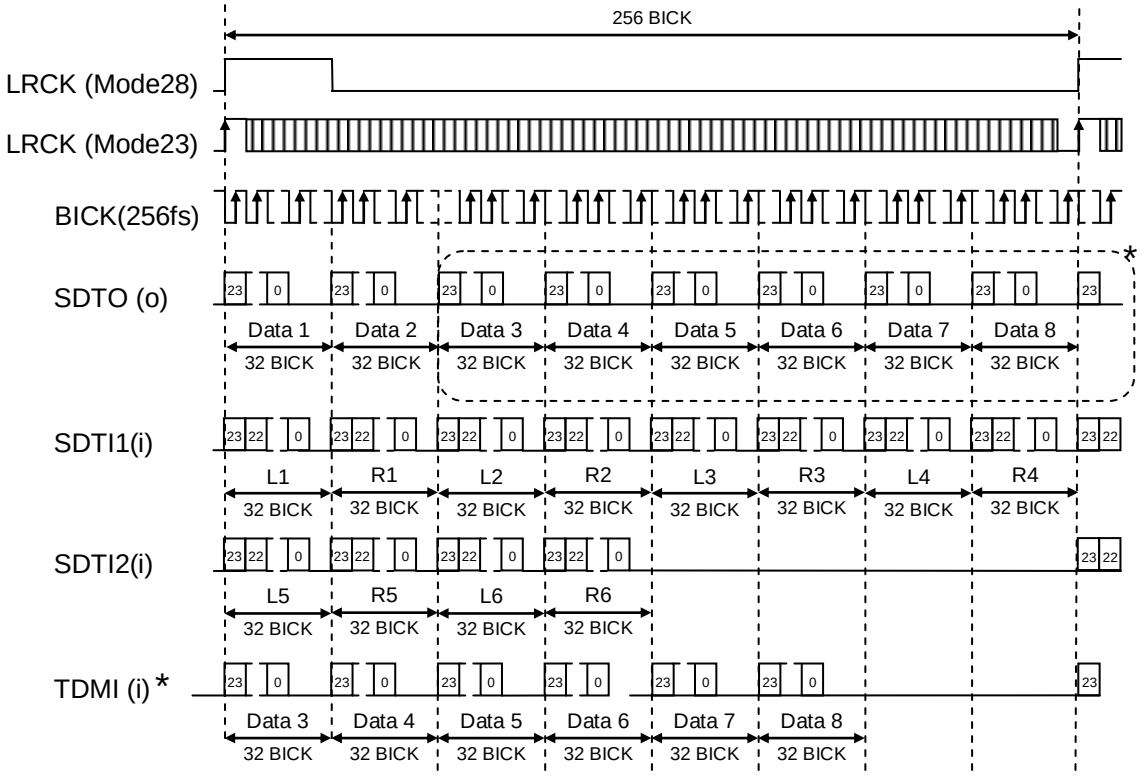


Figure 27. Mode 21/26 Timing (TDM256 Mode)



(*: Optional)

Figure 28. Mode 22/27 Timing (TDM256 Mode)



(*: Optional)

Figure 29. Mode 23/28 Timing (TDM256 Mode)

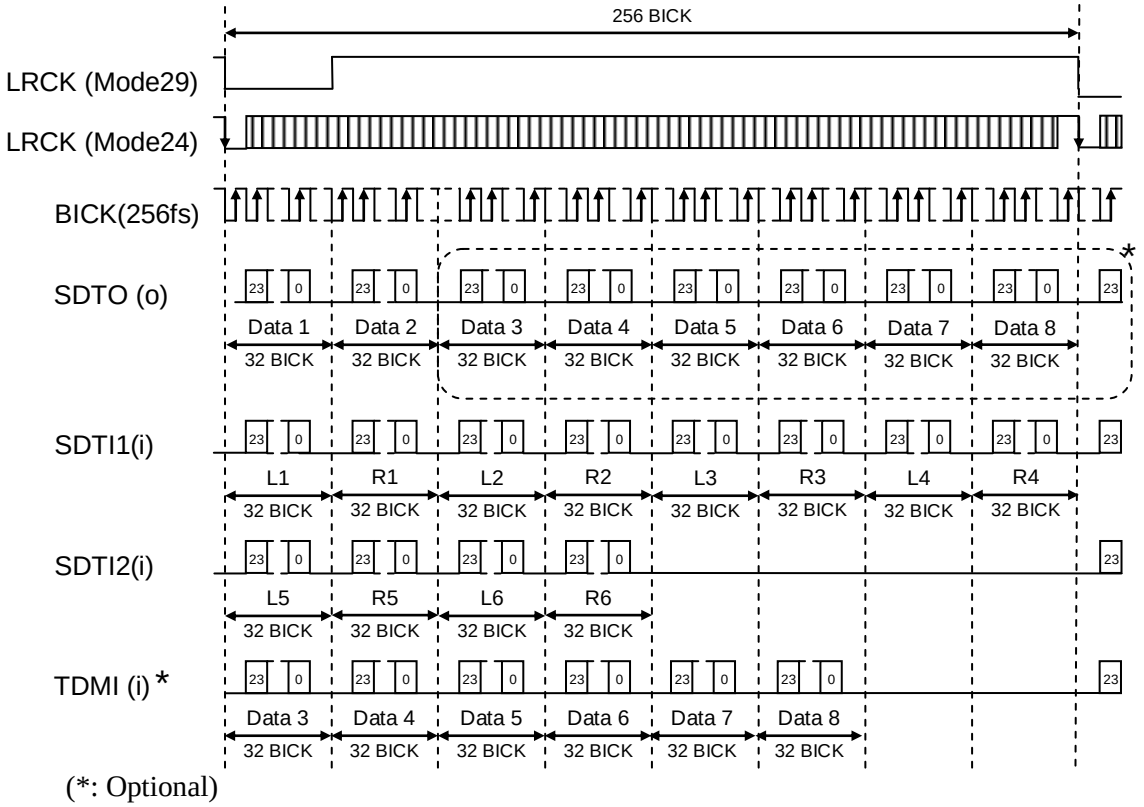


Figure 30. Mode 24/29 Timing (TDM256 Mode)

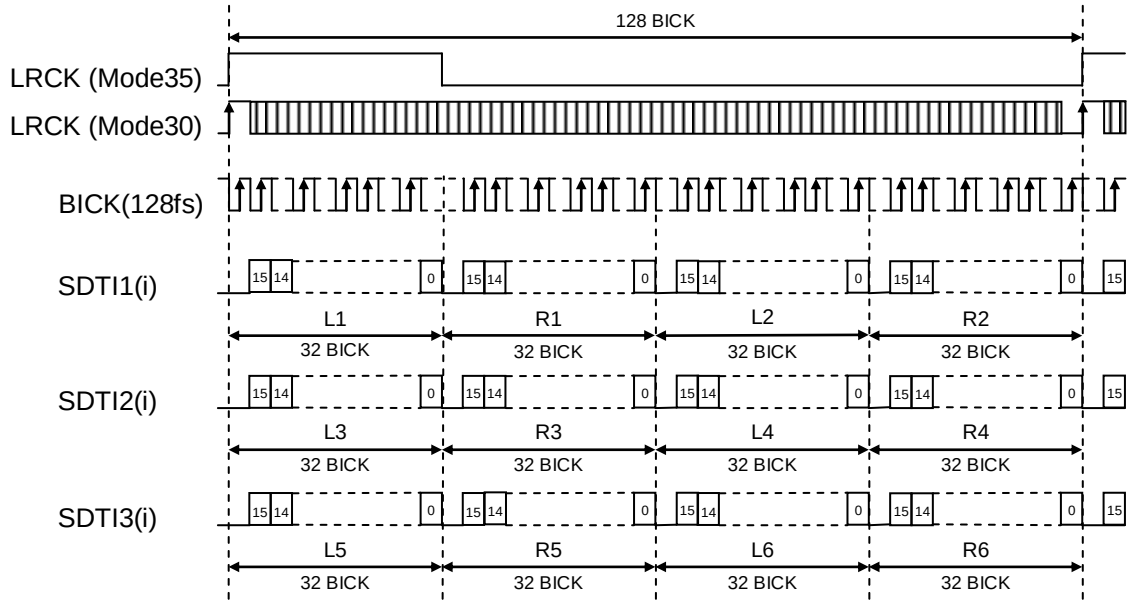


Figure 31. Mode 30/35 Timing (TDM128 Mode)

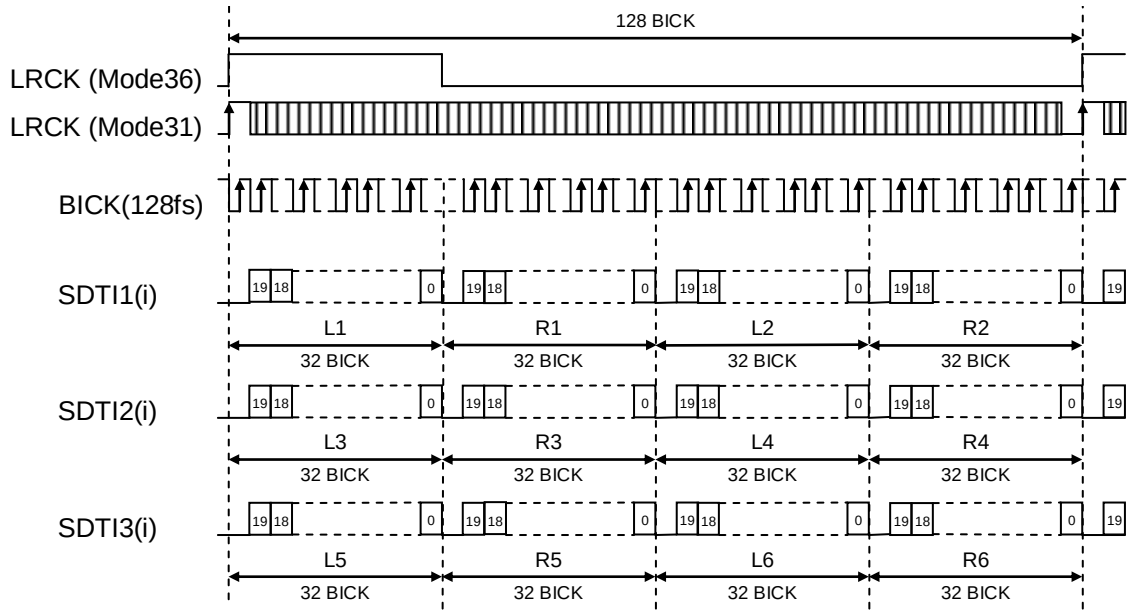


Figure 32. Mode 31/36 Timing (TDM128 Mode)

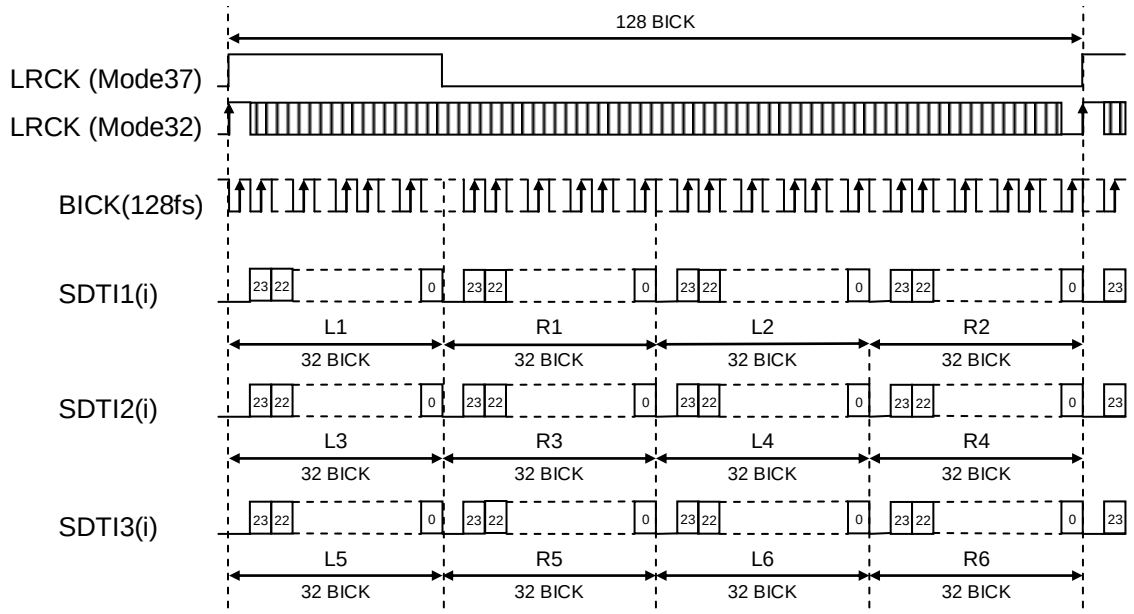


Figure 33. Mode 32/37 Timing (TDM128 Mode)

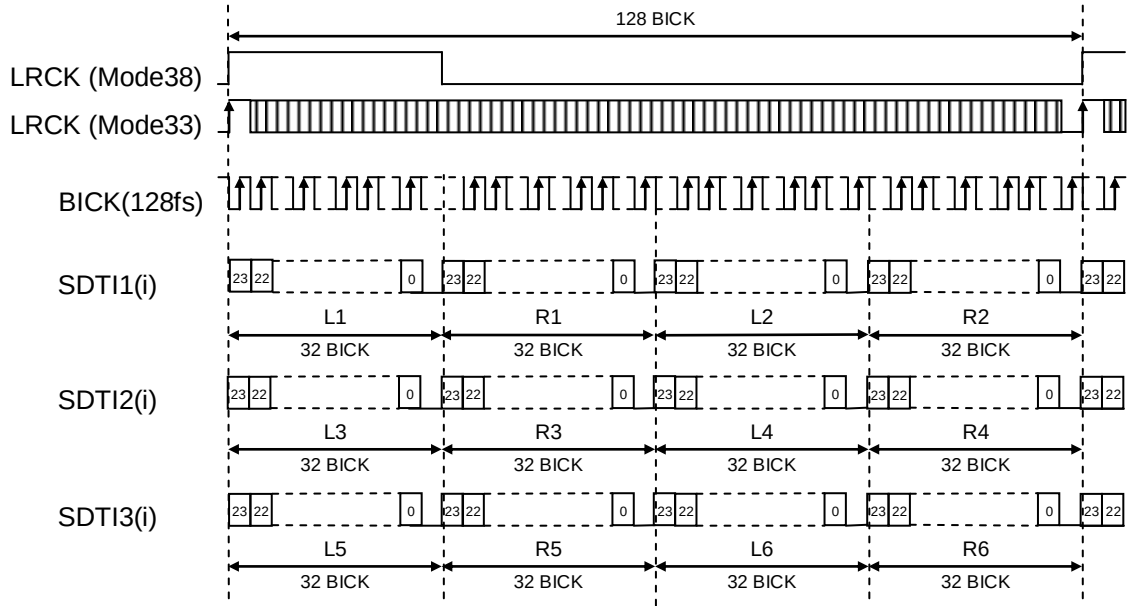


Figure 34. Mode 33/38 Timing (TDM128 Mode)

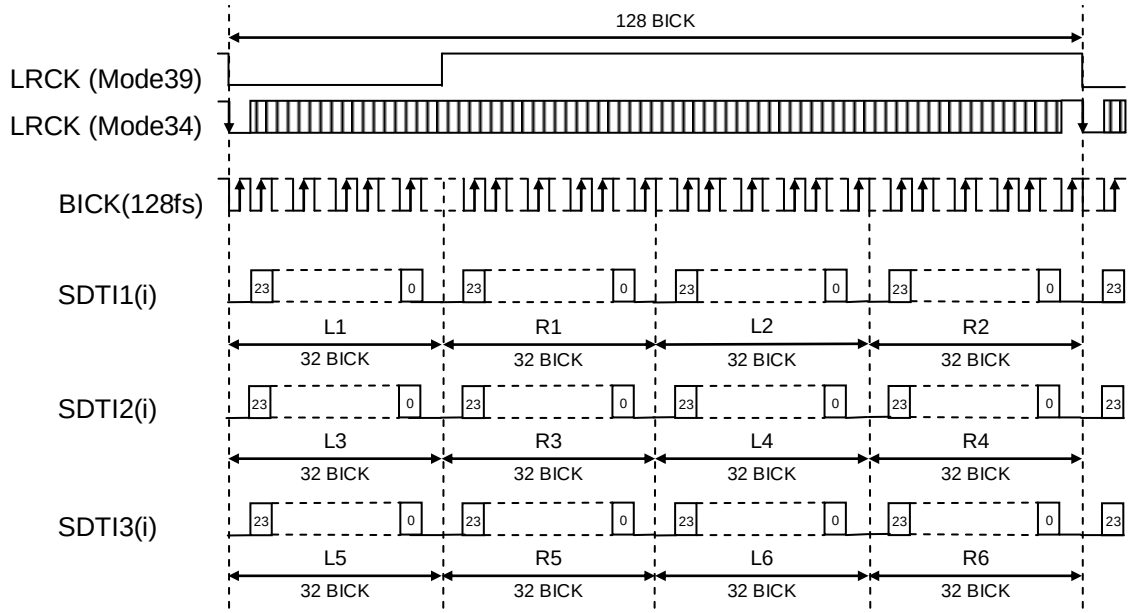


Figure 35. Mode 34/39 Timing (TDM128 Mode)

■ TDM Cascade Mode

The AK4617 can be connected with other ADCs or CODECs in cascades in TDM mode. In Figure 36, the SDTO pin of ADC or CODEC is connected with the TDMI pin of the AK4617. It is possible to output 8channel TDM data from the SDTO pin of the AK4617 as shown in Figure 26 and Figure 30 in TDM256 mode, and it is possible to output 16channel TDM data in TDM 512 mode.

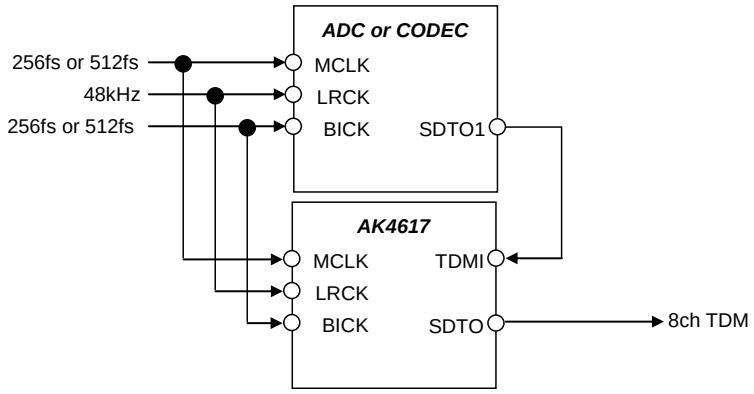


Figure 36. Cascade TDM Connection Diagram

■ Digital Attenuator

AK4617 has a channel-independent digital attenuator (256 levels, 0.5dB steps). Attenuation level of each DAC1-6 can be set by DAATL1/R1 7-0 bit, DAATL2/R2 7-0 bit, DAATL3/R3 7-0 bit, DAATL4/R4 7-0 bit, DAATL5/R5 7-0 bit, DAATL6/R6 7-0 bit, respectively (Table 14).

DAATL1/R1 7-0bit DAATL2/R2 7-0 bit DAATL3/R3 7-0 bit DAATL4/R4 7-0 bit DAATL5/R5 7-0 bit DAATL6/R6 7-0 bit	Attenuation Level	
00H	+0dB	(default)
01H	-0.5dB	
02H	-1.0dB	
:	:	
7DH	-62.5dB	
7EH	-63.0dB	
7FH	-63.5dB	
:	:	
FEH	-127.0dB	
FFH	MUTE (-∞)	

Table 14. Attenuation level of DAC Digital Attenuator

Transition time between set values of DAATL1/R1 7-0, DAATL2/R2 7-0, DAATL3/R3 7-0, DAATL4/R4 7-0, DAATL5/R5 7-0, DAATL6/R6 bit can be selected by the DAATS1-0 bit (Table 15). Transition between set values is the soft transition in Mode1/2/3 eliminating switching noise in the transition.

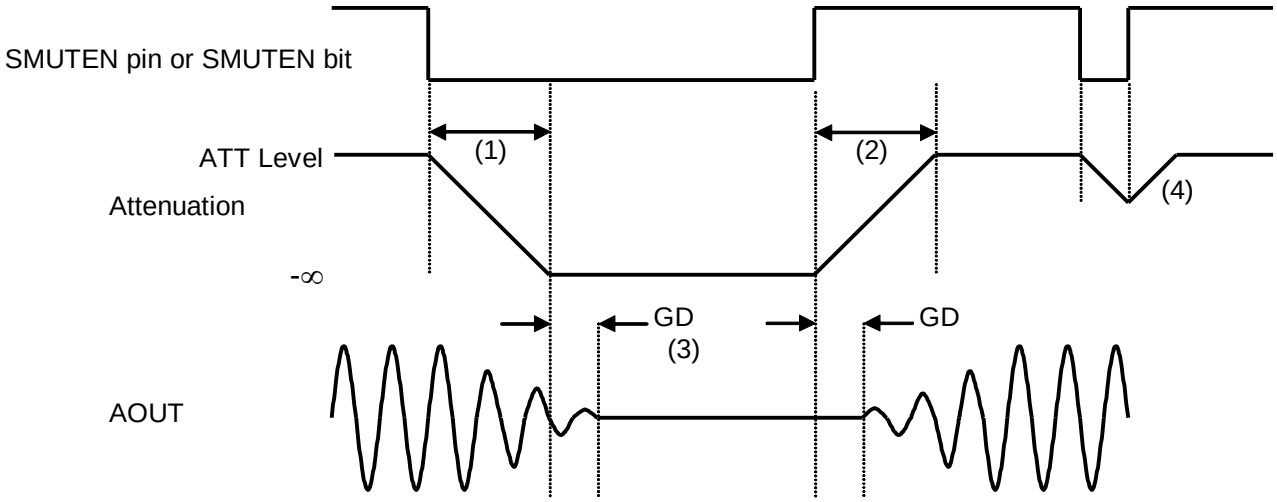
Mode	DAATS1	DAATS0	ATT speed	
0	0	0	4080/fs	(default)
1	0	1	2040/fs	
2	1	0	510/fs	
3	1	1	255/fs	

Table 15. Transition Time between Set Values of DAATL1/R1 7-0, DAATL2/R2 7-0, DAATL3/R3 7-0, DAATL4/R4 7-0, DAATL5/R5 7-0, DAATL6/R6 7-0 bit

The transition between set values is a soft transition of 4080 levels in mode 0. It takes 4080/fs (85ms@fs=48kHz) from 00H to FFH. If the PDN pin goes to "L", DAATL1/R1 7-0, DAATL2/R2 7-0, DAATL3/R3 7-0, DAATL4/R4 7-0, DAATL5/R5 7-0, DAATL6/R6 7-0 bit are initialized to 00H. These bit are also set to 00H respectively when RSTN bit = "0", and fade to their current value when RSTN bit returns to "1".

■ Soft Mute Operation

Soft mute operation is performed in the digital domain. When the SMUTEN pin is set to "L" or SMUTEN bit is set "0", the output signal is attenuated to -∞ in the cycle set by ATS bit (Table 15) from the current ATT level. When the SMUTEN pin is return to "H" or SMUTEN bit is returned to "1", the mute is cancelled and the output attenuation gradually changes to the ATT level in the cycle set by ATS bit. If the soft mute is cancelled before attenuating to -∞ after starting the operation, attenuation is discontinued and it is returned to ATT level by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) The time for input data attenuation to -∞ (Table 15). For example, this time is 4080LRCK cycles (4080/fs) at ATT_DATA=00H. ATT transition of the soft-mute is from 00H to FFH

(2) The time for input data recovery to ATT level (Table 15). For example, this time is 4080LRCK cycles (4080/fs) at ATT-DATA=FFH. ATT transition of soft-mute is from FFH to 00H.

(3) The analog output corresponding to the digital input has group delay, GD.

(4) If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle.

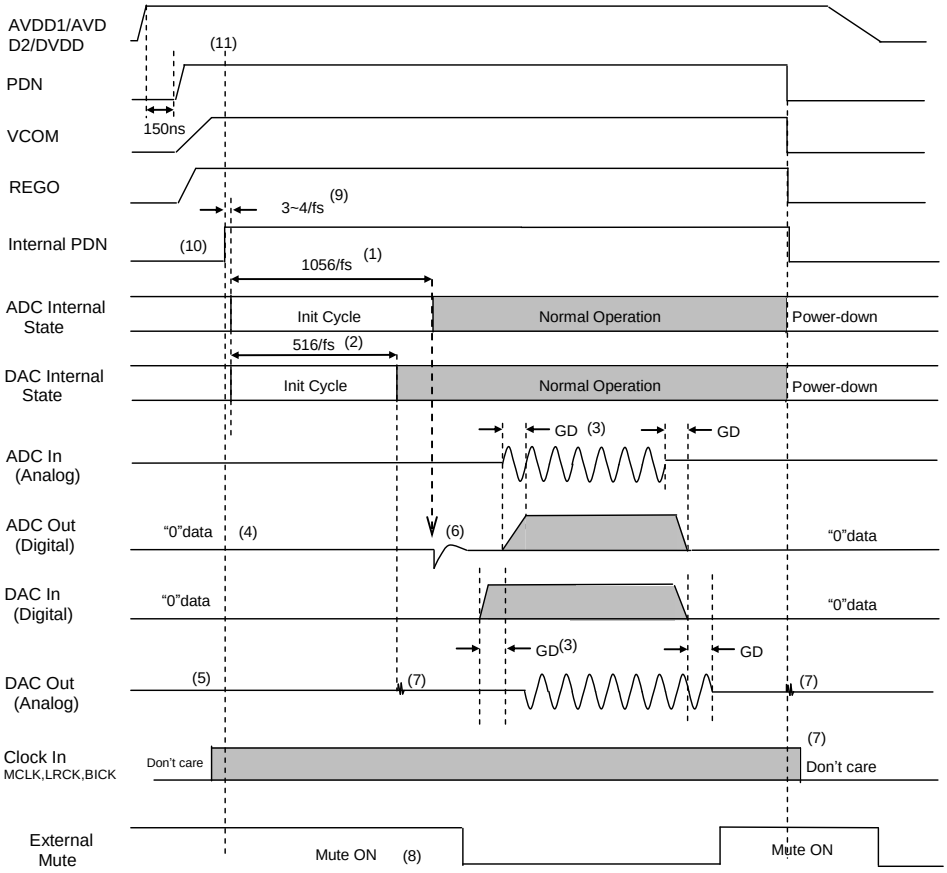
Figure 37. Soft Mute

■ System Reset

The AK4617 should be reset once by bringing the PDN pin = "L" upon power-up. The AK4617 is powered up and the internal timing starts clocking by MCLK or LRCK "↑" after exiting the power down state of reference voltage (such as VCOM) by the PDN pin. The AK4617 is in power-down mode until MCLK and LRCK, BICK are input.

■ Power-Down

All ADCs and DACs of the AK4617 are placed in power-down mode by bringing the PDN pin "L" which resets both digital filters at the same time. The PDN pin "L" also resets the control registers to their default values. In power-down mode, the SDTO goes to "L", and the analog outputs go to Hi-Z. This reset should always be executed after power-up. For the ADC, an analog initialization cycle (1056/fs) starts 3~4/fs after exiting power-down mode. The output data, SDTO is available after 1059~1060 cycles of the LRCK clock. For the DAC, an analog initialization cycle (516/fs) starts 3~4/fs after exiting power-down mode. The analog outputs go to Hi-Z during the initialization. Figure 38 shows the power-down and power-up sequences.



Notes:

(1) The analog part of ADC is initialized after exiting internal power-down state.
When start-up the AK4617, ADC input voltage should be operating common voltage.
It is necessary to wait for the charge up time of HPF which consists of analog inputs.
When the external capacitor is 1uF and the input impedance is 60kΩ(typ), τ = 0.06 sec.

(2) The analog part of DAC is initialized after exiting internal power-down state.

(3) Digital output corresponds to analog input and analog output corresponds to digital input have group delay (GD).

(4) ADC output is "0" data at power-down state.

(5) The analog outputs go to Hi-Z in power-down mode.

(6) Click noise occurs at the end of initialization of the analog part. Mute the digital output externally.

(7) Click noise occurs at the falling edge of PDN and at 519~520/fs after exiting internal power-down state.

(8) Mute the analog output externally.

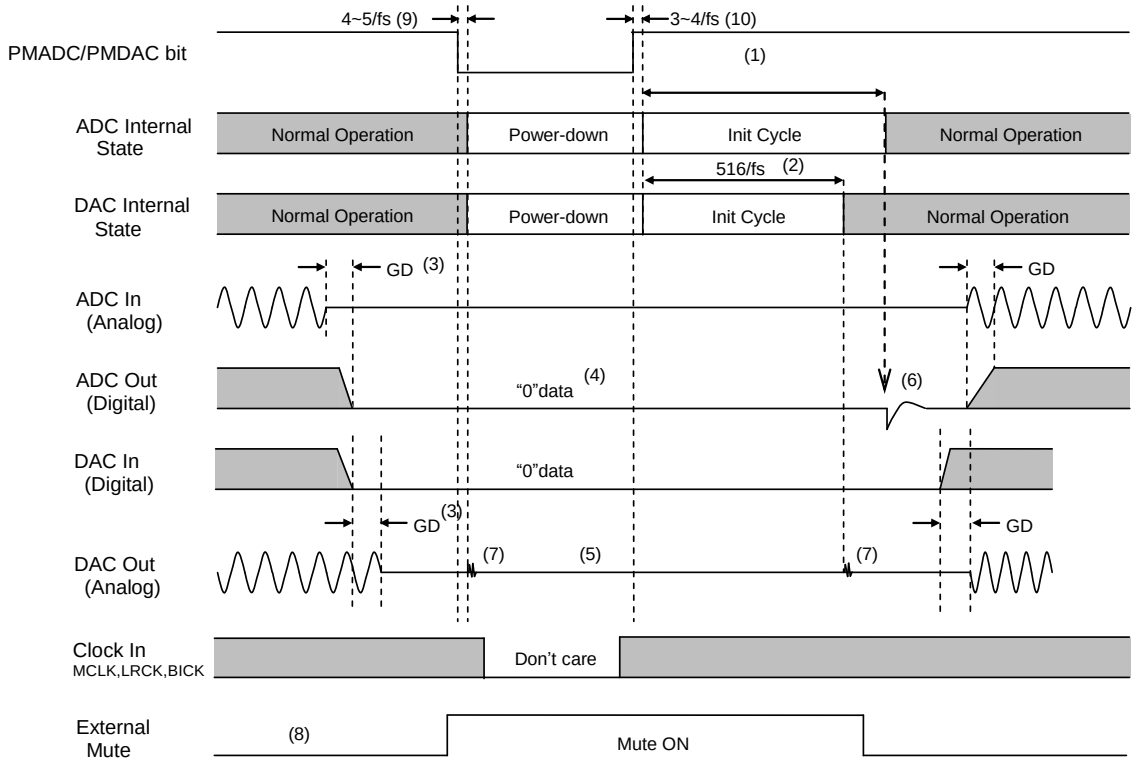
(9) There is a delay, 3~4/fs from internal power up to the start of initial cycle.

(10) The PDN pin must be "L" when power up the AK4617 and set to "H" after all poweres are supplied.

(11) The internal power-down state is released when MCLK counter rise.Do not write to the registers for 32768/MCLK(2.67ms@MCLK=12.288MHz, until internal power down is released after the PDN pin = "H".

Figure 38. Pin power-down/Pin Power-up Sequence Example

All ADCs and all DACs can be powered-down individually through the PMADC bit and PMDAC bit. DAC1-6 can be power-down individually by PMDA6-1 bit. In this case, the internal register values are not initialized. When PMADC bit = "0", SDTO goes to "L". When PMDAC bit = "0", the analog outputs go to Hi-Z. As some click noise occurs, the analog output should be muted externally if the click noise influences system applications. Figure 39 shows the power-down and power-up sequences.



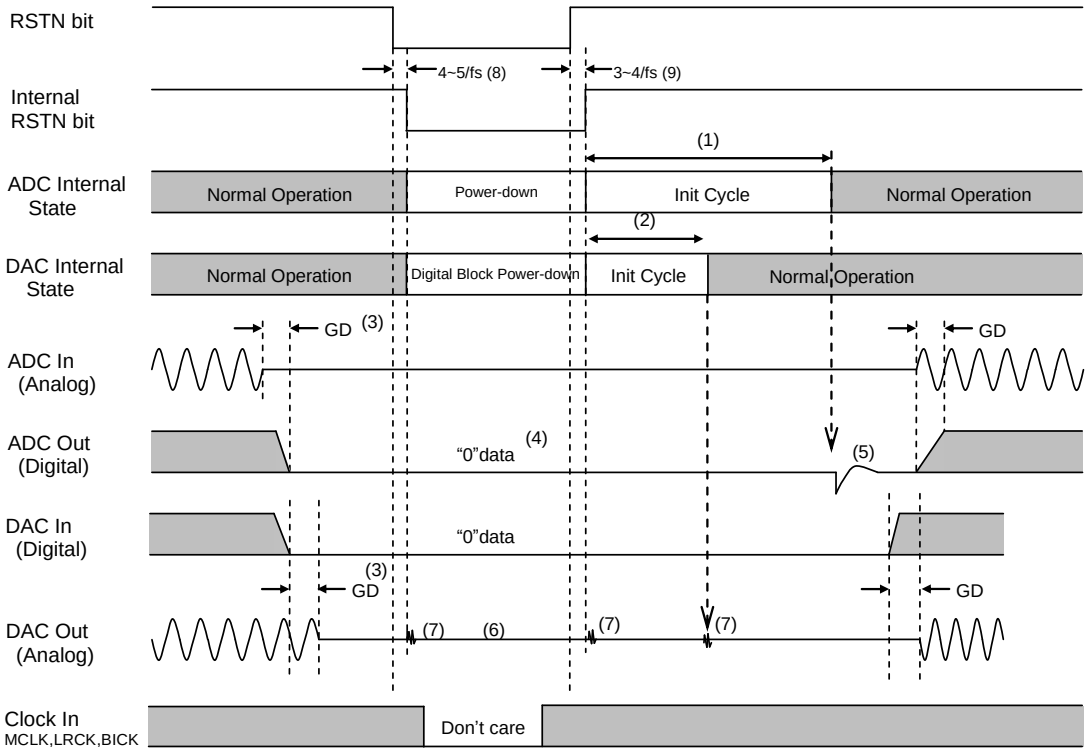
Notes:

(1) The analog section of ADC is initialized after exiting power-down state.
(2) The analog section of DAC is initialized after exiting power-down state.
(3) Digital output corresponding to the analog inputs and analog outputs corresponding to the digital inputs have group delay (GD).
(4) ADC output is "0" data at power-down state.
(5) DAC output is Hi-Z in power-down state.
(6) Click noise occurs at the end of initialization of the analog part. Mute the digital output externally.
(7) Click noise occurs at 4~5/fs after PMDAC bit becomes "0", and occurs at 519~520/fs after PMDAC bit becomes "1".
(8) Mute the analog output externally.
(9) There is a delay, 4~5/fs from PMDAC bit becomes "0" to the applicable ADC power-down.
There is a delay, 4~5/fs from PMDAC bit becomes "0" to the applicable DAC power-down.
(10) There is a delay, 3~4/fs from PMADC and PMDAC bit become "1" to the start of initial cycle.

Figure 39. Bit power-down/Bit power-up sequence example

■ Reset Function

When RSTN bit= "0", the analog and digital part of ADC and DACs are powered-down, but the internal register are not initialized. The analog outputs go to Hi-Z, the SDTO pin goes to "L". As some click noise occurs, the analog output should be muted externally if the click noise influences system application. Figure 40 shows the power-up sequence.



Notes:

(1) The analog section of the ADC is initialized after exiting reset state.
The initializing cycle is 1056fs. When start-up the AK4617, ADC input voltage should be operating common voltage.

(2) The analog section of DAC is initialized after exiting exiting reset state.

(3) Digital output corresponding to the analog inputs, and analog outputs corresponding to the digital inputs have group delay (GD).

(4) ADC output is "0" data at power-down state.

(5) Click noise occurs when the initializing cycle is finished. Mute the digital output externally.

(6) The analog outputs go to Hi-Z when RSTN bit becomes "0".

(7) Click noise occurs at 4~5/fs after RSTN bit becomes "0", and it occurs at 3~4/fs after RSTN bit becomes "1".

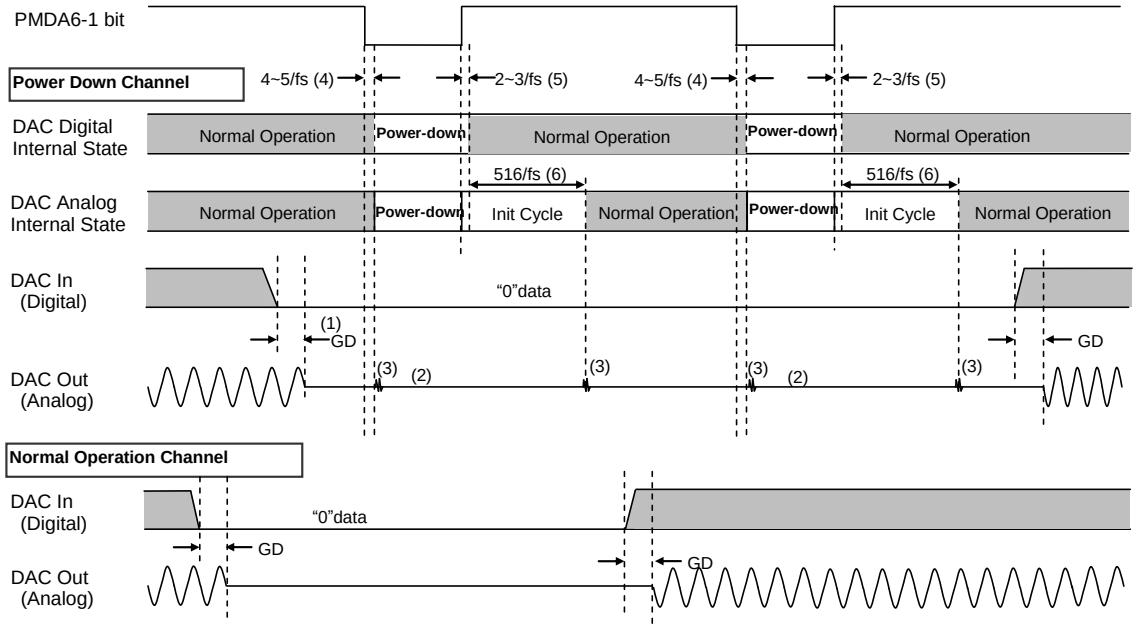
(8) There is a delay, 4~5/fs from RSTN bit "0" to the internal RSTN bit "0".

(9) There is a delay, 3~4/fs from RSTN bit "1" to the start of initial cycle.

Figure 40. Reset Sequence Example

■ DAC Partial Power-Down Function

All of the DACs can be powered-down individually by PMDA6-1 bit. The analog section and the digital section of the DAC are placed in power-down mode when the PMDA6-1 bit = "0". The analog output of the powered-down channels, which are set by PMDA6-1 bit, go to Hi-Z. Some click noise occurs in both set-up and release of power-down. Mute the analog output externally or set PMDA6-1 bit when PMDAC bit = "0" or RSTN bit = "0". Figure 41 shows the sequence of the power-down and the power-up by PMDA6-1 bit.



Notes:

(1) Analog outputs corresponding to the digital inputs have group delay (GD).
(2) Analog output of the DAC is powered down by PMDA6-1 = "0" and goes to Hi-Z.
(3) Click noise occurs in 4~5/fs after PMDA6-1 bit are set to "0", and it occurs in 518~519/fs after PMDA6-1 bit are set to "1".
(4) The DACs will be powered-down 4~5fs after PMDA6-1 bit = "0"
(5) The initialization stars 2~3fs after PMDA6-1 bit are set to "1".
(6) The analog parts of DACs are initialized after exiting power down mode.

Figure 41. DAC Partial Power-down Example

■ Parallel Mode

The AK4617 can be in parallel mode which does not use internal registers by setting the SPI pin = "L" and PS pin= "H". The parallel mode operation is set by the MS, TDM0, and DIF pins. The AK4617 cannot be changed to Serial mode from parallel mode during operation.

MS pin	TDM0 pin	DIF pin	Mode	MS, TDM0, DIF2/1/0
L	L	L	Mode3 (Table 10)	00011
L	L	H	Mode4 (Table 10)	00100
H	L	L	Mode8 (Table 10)	10011
H	L	H	Mode9 (Table 10)	10100
L	H	L	Mode13 (Table 11)	01011
L	H	H	Mode14 (Table 11)	01100
H	H	L	Mode18 (Table 11)	11011
H	H	H	Mode19 (Table 11)	11100

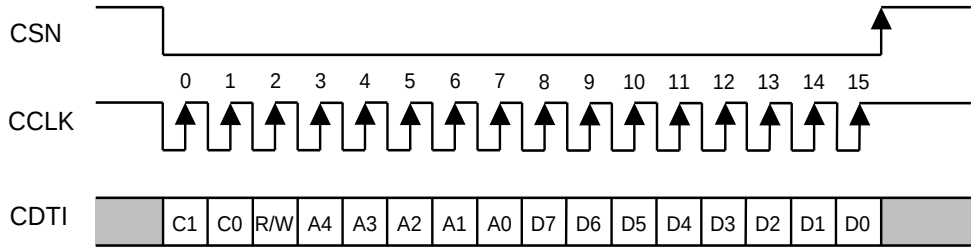
■ Serial Control Interface

The AK4617's functions are controlled through registers or pins. The registers may be written by two types of control modes. The chip address is determined by the state of the CAD1 input. The PDN pin = "L" initializes the registers to their default values. Writing "0" to the RSTN bit can initialize the internal timing circuit, but the register data will not be initialized. *When the PDN pin = "L", control register writings are not valid.

(1) 3-wire Serial Control Mode (SPI pin = "H")

The internal registers may be written through the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a 2-bit Chip address, Read/Write (1bit, Fixed to "1", Write only), Register address (MSB first, 5-bit) and Control data (MSB first, 8-bit). The chip address high bit is set by the CAD1 pin and the lower bit is fixed to "0". Address and data are clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after a low-to-high transition of CSN. The clock speed of CCLK is 5MHz(max).

* The AK4617 does not support read commands in 3wire serial control mode.



C1-C0: Chip Address (C1=CAD1 pin, C0= "L")
R/W: Read/Write (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 42. 3-wire Serial Control I/F Timing

(2) I²C-bus Control Mode (SPI pin = "L", PS pin ="L")
The AK4617 supports the fast-mode I²C-bus (max: 400kHz).

1. WRITE Operations
Figure 43 shows the data transfer sequence of the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 49). After the START condition, a slave address is sent. This address is 7-bit long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bit is CAD1 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD1 pin) sets these device address bit (Figure 44). If the slave address matches that of the AK4617, the AK4617 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 50). R/W bit = "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4617. The format is MSB first, and those most significant 3-bit are fixed to zeros (Figure 45). The data after the second byte contains control data. The format is MSB first, 8-bit (Figure 46). The AK4617 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 49).

The AK4617 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4617 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 13H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 51) except for the START and STOP conditions.

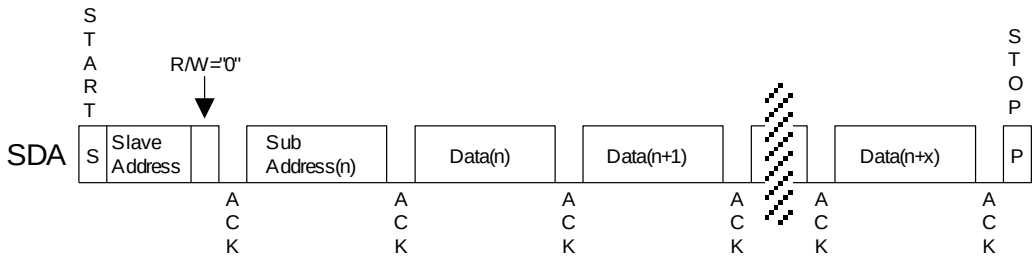


Figure 43. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	CAD1	0	R/W

(That CAD1 should match with CAD1 pin)
Figure 44. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 45. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 46. Byte Structure after the second byte

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4617. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 0EH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 13H will be read out.

The AK4617 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK4617 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4617 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4617 ceases transmission.

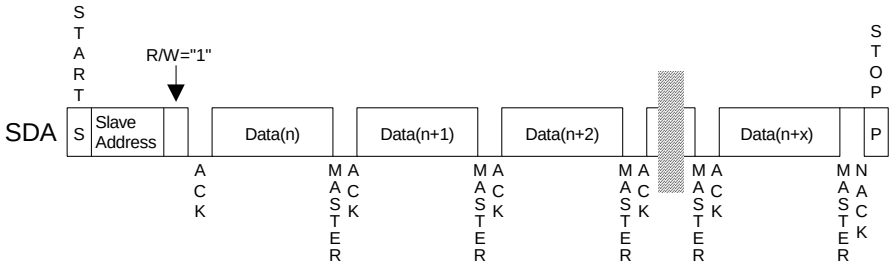


Figure 47. CURRENT ADDRESS READ

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit ="1", the master must execute a "dummy" write operation first. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit ="1". The AK4617 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4617 ceases transmission.

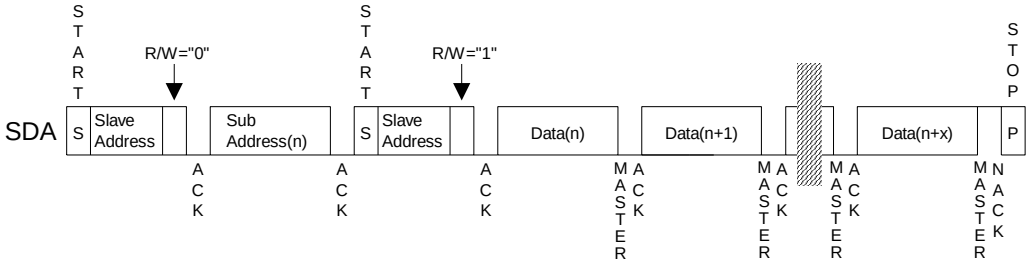


Figure 48. RANDOM ADDRESS READ

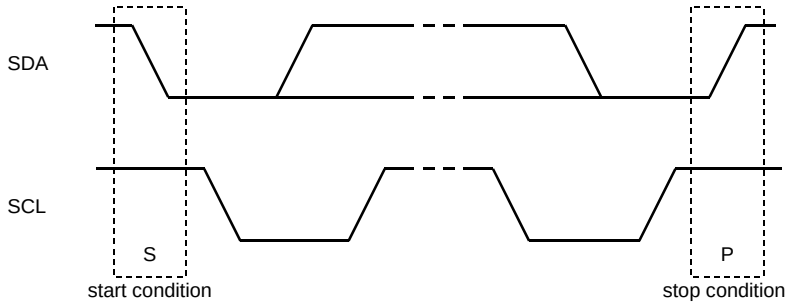


Figure 49. START and STOP Conditions

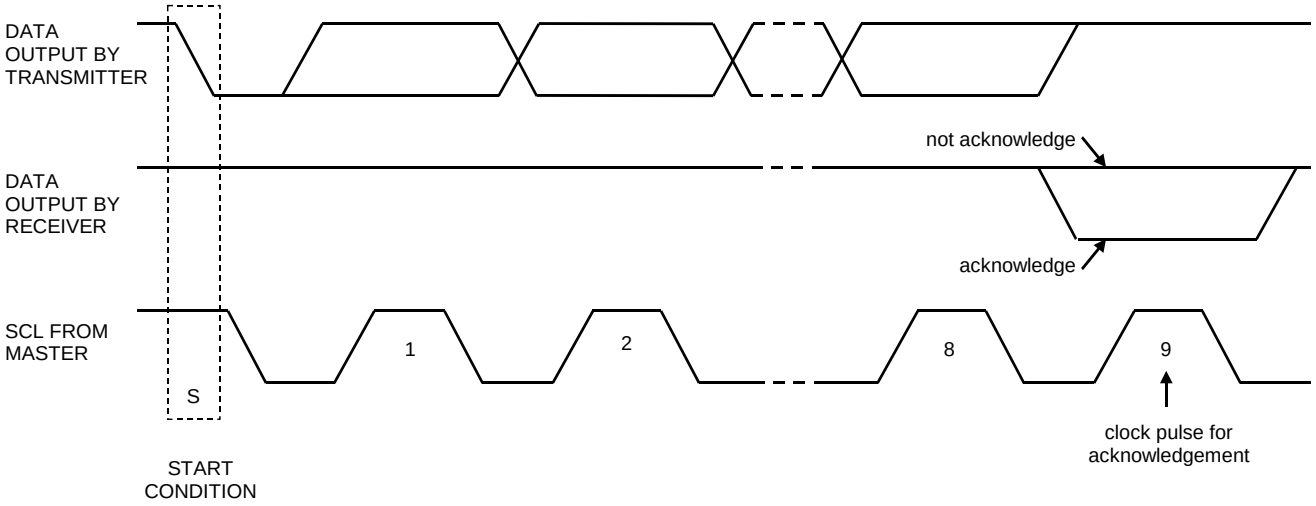


Figure 50. Acknowledge on the I^2C-Bus

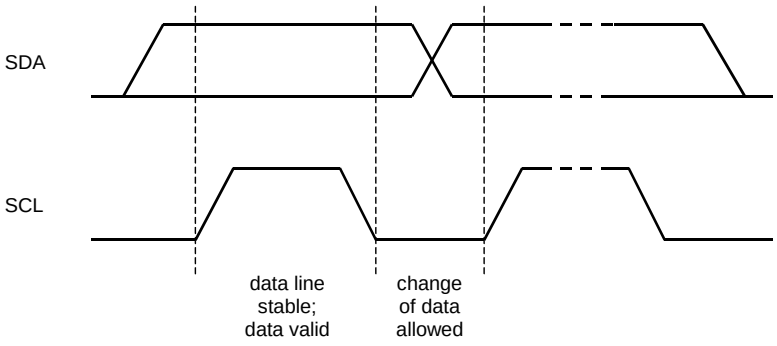


Figure 51. Bit Transfer on the I^2C-Bus

■ Register Map

Add	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	0	PMADC	PMDAC	0	0	MS	RSTN
01H	Power Management 2	0	0	PMDA6	PMDA5	PMDA4	PMDA3	PMDA2	PMDA1
02H	System Clock	CKS1	CKS0	DFS1	DFS0	0	0	0	ACKS
03H	Filter setting1	DEM41	DEM40	DEM31	DEM30	DEM21	DEM20	DEM11	DEM10
04H	Filter setting2	SLOW	SD_DA	0	SD_AD	DEM61	DEM60	DEM51	DEM50
05H	Audio Interface Format	0	0	TDM1	TDM0	0	DIF2	DIF1	DIF0
06H	Soft Mute	0	0	DAATS1	DAATS0	0	0	0	SMUTEN
07H	DAC1L Volume	DAATL17	DAATL16	DAATL15	DAATL14	DAATL13	DAATL12	DAATL11	DAATL10
08H	DAC1R Volume	DAATR17	DAATR16	DAATR15	DAATR14	DAATR13	DAATR12	DAATR11	DAATR10
09H	DAC2L Volume	DAATL27	DAATL26	DAATL25	DAATL24	DAATL23	DAATL22	DAATL21	DAATL20
0AH	DAC2R Volume	DAATR27	DAATR26	DAATR25	DAATR24	DAATR23	DAATR22	DAATR21	DAATR20
0BH	DAC3L Volume	DAATL37	DAATL36	DAATL35	DAATL34	DAATL33	DAATL32	DAATL31	DAATL30
0CH	DAC3R Volume	DAATR37	DAATR36	DAATR35	DAATR34	DAATR33	DAATR32	DAATR31	DAATR30
0DH	DAC4L Volume	DAATL47	DAATL46	DAATL45	DAATL44	DAATL43	DAATL42	DAATL41	DAATL40
0EH	DAC4R Volume	DAATR47	DAATR56	DAATR45	DAATR44	DAATR43	DAATR42	DAATR41	DAATR40
0FH	DAC5L Volume	DAATL57	DAATL56	DAATL55	DAATL54	DAATL53	DAATL52	DAATL51	DAATL50
10H	DAC5R Volume	DAATR67	DAATR66	DAATR55	DAATR54	DAATR53	DAATR52	DAATR51	DAATR50
11H	DAC6L Volume	DAATL67	DAATL66	DAATL65	DAATL64	DAATL63	DAATL62	DAATL61	DAATL60
12H	DAC6R Volume	DAATR67	DAATR66	DAATR65	DAATR64	DAATR63	DAATR62	DAATR61	DAATR60
13H	Input Selector	0	0	0	0	0	0	DIE2	DIE1

Note: For addresses from 14H to 1FH, data must not be written. The bit defined as 0 must contain a “0” value.
When the PDN pin goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the internal timing is reset, but registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	0	PMADC	PMDAC	0	0	MS	RSTN
R/W		RD	RD	R/W	R/W	RD	RD	R/W	R/W
Default		0	0	1	1	0	0	0	1

RSTN: Internal timing reset
0: Reset.
1: Normal operation (default)

MS: Master Mode Select
0: Slave Mode (default)
1: Master Mode

PMDAC: Power management of DAC1-6
0: All DAC's Power-down. PMDA1-6 bit are invalid.
1: Normal operation. (default) PMDA1-6 bit are valid.

PMADC: Power management of ADC
0: ADC's Power-down.
1: Normal operation. (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 3	0	0	PMDA6	PMDA5	PMDA4	PMDA3	PMDA2	PMDA1
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	1	1	1

PMDA6-1: Power management of DAC1-6 (0: Power-down, 1: Normal operation)
PMDA1: Power management control of DAC1
PMDA2: Power management control of DAC2
PMDA3: Power management control of DAC3
PMDA4: Power management control of DAC4
PMDA5: Power management control of DAC5
PMDA6: Power management control of DAC6

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	System Clock	CKS1	CKS0	DFS1	DFS0	0	0	0	ACKS
R/W		R/W	R/W	R/W	R/W	RD	RD	RD	R/W
Default		1	0	0	0	0	0	0	0

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the setting of DFS are ignored. When this bit is "0", DFS0, 1 set the sampling speed mode.

DFS1-0: Sampling speed mode (Table 1)
The setting of DFS is ignored at ACKS bit ="1".

CKS1-0: Master Clock Input Frequency Select (Table 2)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Filter setting1	DEM41	DEM40	DEM31	DEM30	DEM21	DEM20	DEM11	DEM10
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	1	0	1

DEM11-10: De-emphasis response control for DAC1 data on SDTI1 (Table 8)
Initial: "01", OFF

DEM21-20: De-emphasis response control for DAC2 data on SDTI2 (Table 8)
Initial: "01", OFF

DEM31-30: De-emphasis response control for DAC3 data on SDTI3 (Table 8)
Initial: "01", OFF

DEM41-40: De-emphasis response control for DAC4 data on SDTI4 (Table 8)
Initial: "01", OFF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Filter setting2	SLOW	SD_DA	0	SD_AD	DEM61	DEM60	DEM51	DEM50
R/W		R/W	R/W	RD	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	1	0	1

DEM51-50: De-emphasis response control for DAC5 data on SDTI5 (Table 8)
Initial: "01", OFF

DEM61-60: De-emphasis response control for DAC6 data on SDTI6 (Table 8)
Initial: "01", OFF

SD_AD: Digital filter Setting for ADC
0: Sharp roll off filter
1: Short delay Sharp roll off filter (default)

SD_DA: Digital filter Setting for DAC
0: Sharp roll off filter or Slow roll off filter
1: Short delay Sharp roll off filter or Short delay Slow roll off filter (default)

SLOW: Slow Roll-off Filter Enable for DAC
0: Sharp Roll-off Filter (default)
1: Slow Roll-off Filter

SD_DA bit	SLOW bit	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay Sharp roll-off filter	(default)
1	1	Short delay Slow roll-off filter	

Table 16 Digital Filter setting for DAC

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Audio Interface Format	0	0	TDM1	TDM0	0	DIF2	DIF1	DIF0
R/W		RD	RD	R/W	R/W	RD	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

DIF2-0: Audio Data Interface Modes (Table 10, Table 11, Table 12, Table 13)
Initial: "100", mode 4

TDM1-0: TDM Format Select (Table 10, Table 11, Table 12, Table 13)

Mode	TDM1	TDM0	SDTI	Sampling Speed
0	0	0	1-6	Stereo mode (Normal, Double, Quad Speed Mode)
1	0	1	1	TDM512 mode (Normal Speed Mode)
2	1	0	1-2	TDM256 mode (Normal, Double Speed Mode)
3	1	1	1-3	TDM128 mode (Quad Speed Mode)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Soft Mute	0	0	DAATS1	DAATS0	0	0	0	SMUTEN
R/W		RD	RD	R/W	R/W	RD	RD	RD	R/W
Default		0	0	0	0	0	0	0	1

SMUTEN: Soft Mute Enable

SMUTEN pin	SMUTEN bit	All Analog Outputs Status	
L	0	Mute	
	1	Mute	(default)
H	0	Mute	
	1	Unmute	(default)

Table 17. Soft Mute Control

DAATS1-0: DAC Digital attenuator transition time setting (Table 15)
Initial: "00", mode 0

Add	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	DAC1L Volume	DAATL17	DAATL16	DAATL15	DAATL14	DAATL13	DAATL12	DAATL11	DAATL10
08H	DAC1R Volume	DAATR17	DAATR16	DAATR15	DAATR14	DAATR13	DAATR12	DAATR11	DAATR10
09H	DAC2L Volume	DAATL27	DAATL26	DAATL25	DAATL24	DAATL23	DAATL22	DAATL21	DAATL20
0AH	DAC2R Volume	DAATR27	DAATR26	DAATR25	DAATR24	DAATR23	DAATR22	DAATR21	DAATR20
0BH	DAC3L Volume	DAATL37	DAATL36	DAATL35	DAATL34	DAATL33	DAATL32	DAATL31	DAATL30
0CH	DAC3R Volume	DAATR37	DAATR36	DAATR35	DAATR34	DAATR33	DAATR32	DAATR31	DAATR30
0DH	DAC4L Volume	DAATL47	DAATL46	DAATL45	DAATL44	DAATL43	DAATL42	DAATL41	DAATL40
0EH	DAC4R Volume	DAATR47	DAATR56	DAATR45	DAATR44	DAATR43	DAATR42	DAATR41	DAATR40
0FH	DAC5L Volume	DAATL57	DAATL56	DAATL55	DAATL54	DAATL53	DAATL52	DAATL51	DAATL50
10H	DAC5R Volume	DAATR67	DAATR66	DAATR55	DAATR54	DAATR53	DAATR52	DAATR51	DAATR50
11H	DAC6L Volume	DAATL67	DAATL66	DAATL65	DAATL64	DAATL63	DAATL62	DAATL61	DAATL60
12H	DAC6R Volume	DAATR67	DAATR66	DAATR65	DAATR64	DAATR63	DAATR62	DAATR61	DAATR60
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DAATL1/R1 7-0, DAATL2/R2 7-0, DAATL3/R3 7-0, DAATL4/R4 7-0, DAATL5/R5 7-0, DAATL6/R6 7-0: Attenuation Level (Table 14)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Input Selector	0	0	0	0	0	0	DIE2	DIE1
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

DIE2-1: Single-ended/Differential Input Select

0: Single-ended input to the IN1/IN1P and IN2/IN2P pins. Leave the IN1N and IN2N pins open. (default)

1: Differential Input (IN1P/IN2P and IN1N/IN2N pins)

16. Recommended External Circuits

Figure 52, Figure 53 and Figure 54 show the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

- 3-wire Serial Control Mode (SPI pin = "H").
- Slave Mode (MS bit = "0").
- Single-ended Input Mode (DIE2-1 bit = "00")

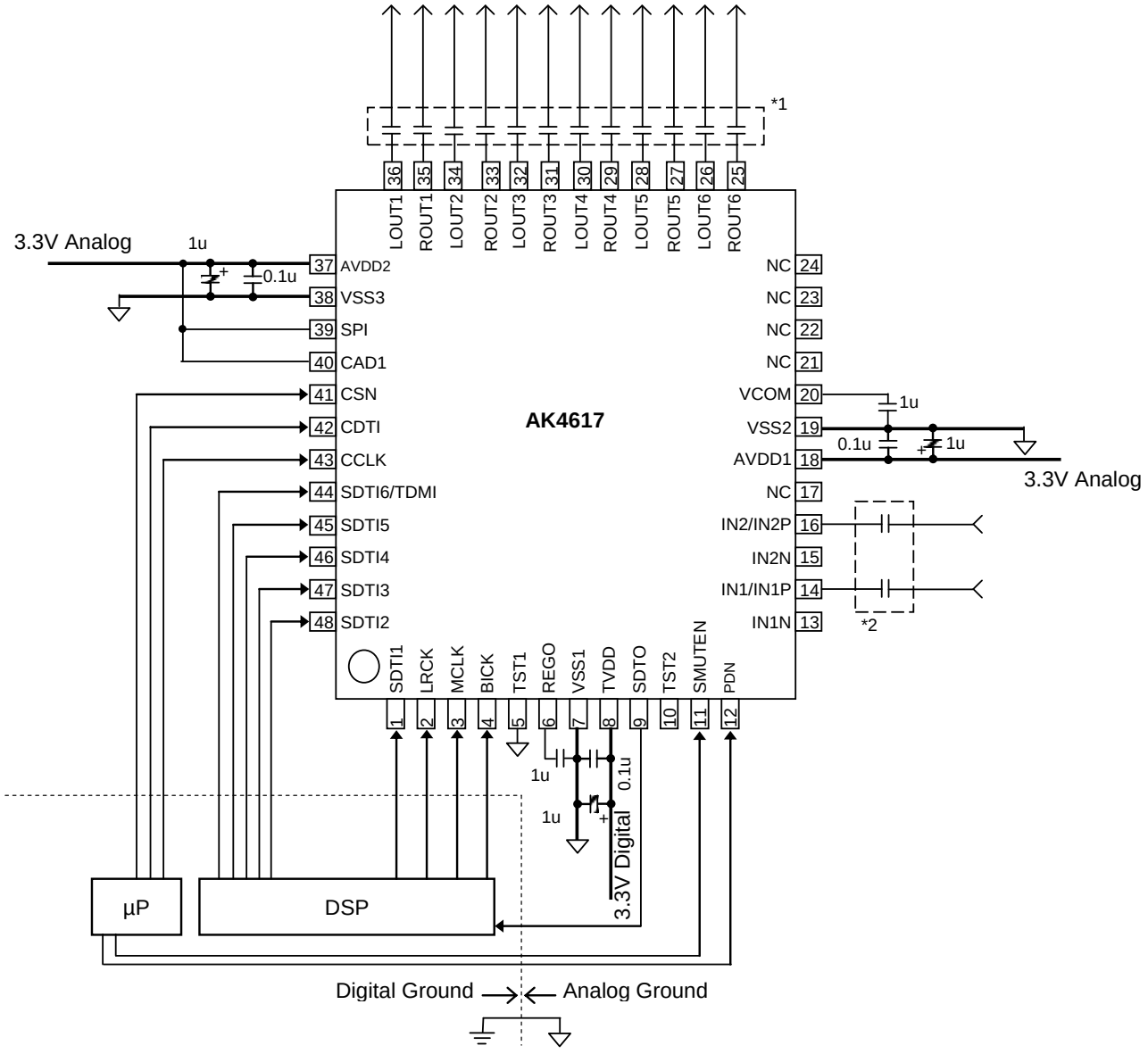


Figure 52. Typical Connection Diagram1 (SPI mode)

*1: Refer to Figure 57.
*2: Refer to Figure 55 and Figure 56.

- 3-wire Serial Control Mode (SPI pin = "L").
- Slave Mode (MS bit = "0").
- Single-ended Input Mode (DIE2-1 bits = "00")
- I^{2}C Bus serial control mode (PS pin = "L")

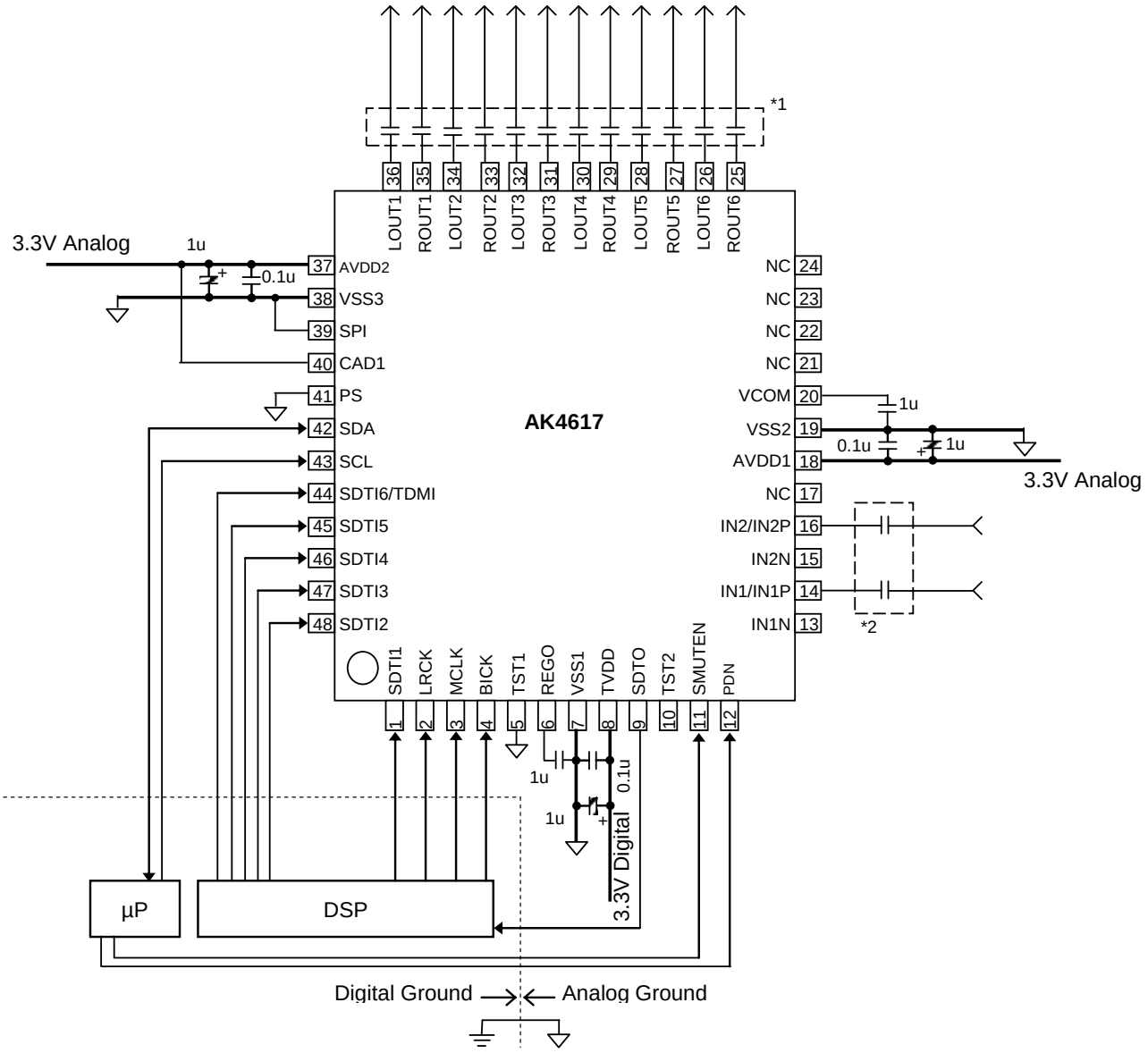


Figure 53. Typical Connection Diagram2 (I^{2}C mode)

*1: Refer to Figure 57.
*2: Refer to Figure 55 and Figure 56.

- 3-wire Serial Control Mode (SPI pin = "L").
- Slave Mode (MS pin = "L").
- Single-ended Input Mode (DIE2-1 bits = "00")
- Parallel Control Mode (PS pin = "H")
- Normal I/F Format Mode (TDM pin = "L")
- 24-bit I^{2}S Mode (DIF pin = "H")

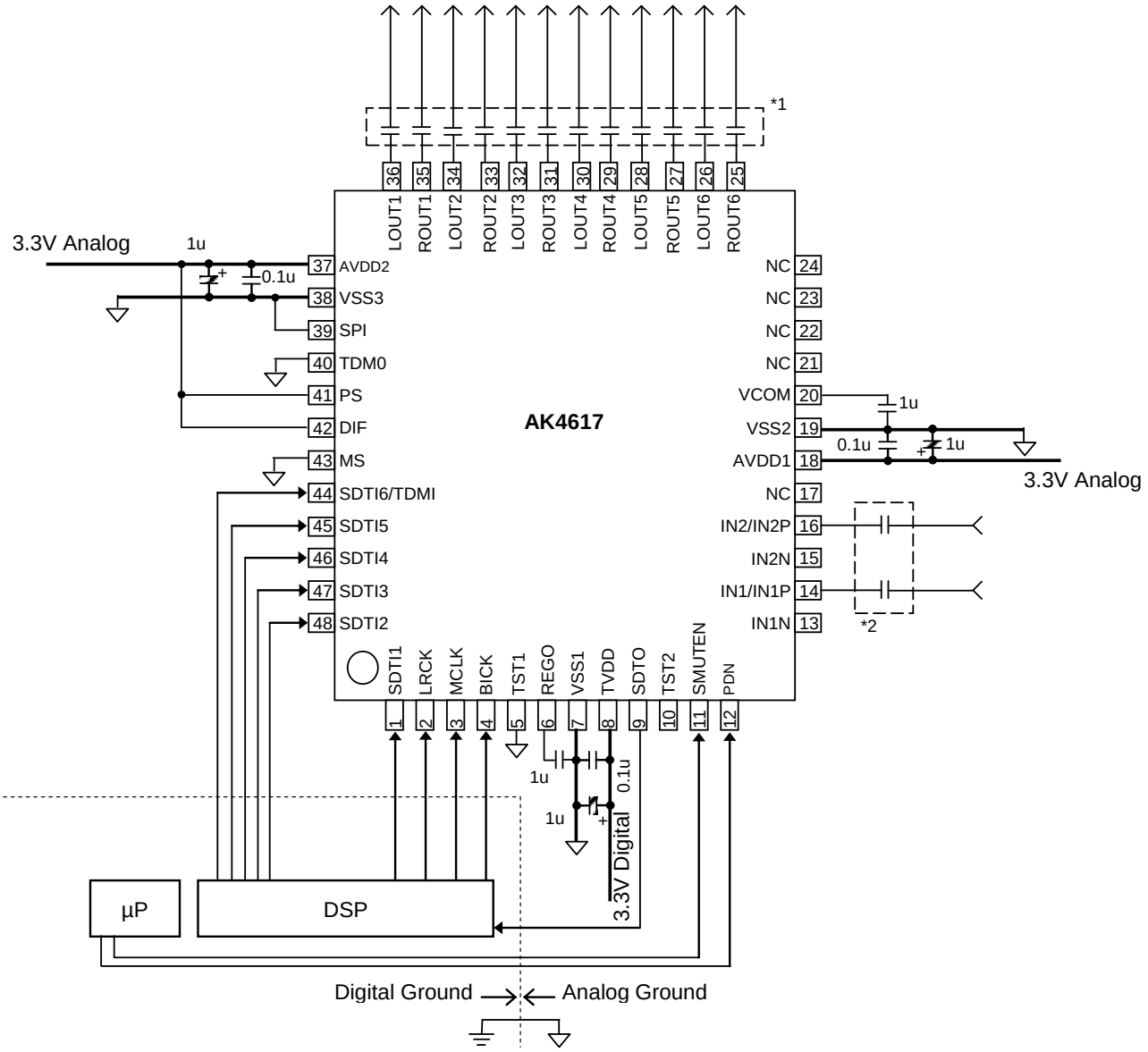


Figure 54. Typical Connection Diagram3 (Parallel mode)

*1: Refer to Figure 57.
*2: Refer to Figure 55 and Figure 56.

■ Grounding and Power Supply Decoupling

The AK4617 requires careful attention to power supply and grounding arrangements. AVDD1, AVDD2 and TVDD are usually supplied from analog supply in system. Alternatively if AVDD1, AVDD2 and TVDD are supplied separately, the power up sequence is not critical. **VSS1 ~ 3 of the AK4617 must be connected to analog ground plane.** System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4617 as possible, with the small value ceramic capacitor being the nearest.

■ Voltage Reference

VCOM is a signal ground of this chip and output the voltage AVDD1x1/2. A ceramic capacitor 1μF attached to the VCOM pin eliminates the effects of high frequency noise. This capacitor should be as close to the pin as possible. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4617.

■ Analog Inputs

The Stereo ADC supports both single-ended and differential inputs. The single-ended input signal range scales with the supply voltage and nominally 0.81xAVDD1 Vpp (typ). The differential input signal range between IN+ and IN− scales with the supply voltage and nominally ±0.81xAVDD1 Vpp (typ). The power supply voltage range of the AK4617 is from VSS2 to AVDD1. The ADC output data format is 2's complement. The internal HPF removes the DC offset.

The AK4617 samples the analog inputs at 64fs (@ fs=48kHz). The digital filter removes noise above the stop band except for multiples of the sampling frequency of analog inputs. The AK4617 includes an anti-aliasing filter (RC filter) to attenuate a noise around the sampling frequency of analog inputs.

■ Analog Outputs

The single-ended output signal range is nominally 0.76 x AVDD2 Vpp centered around the VCOM voltage. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband, in single-ended input mode. There are no internal analog filters for differential output mode, therefore this noise should be removed by the external analog filters.

The DAC outputs have DC offsets of a few millivolts to VCOM voltage.

■ External Analog Inputs Circuit

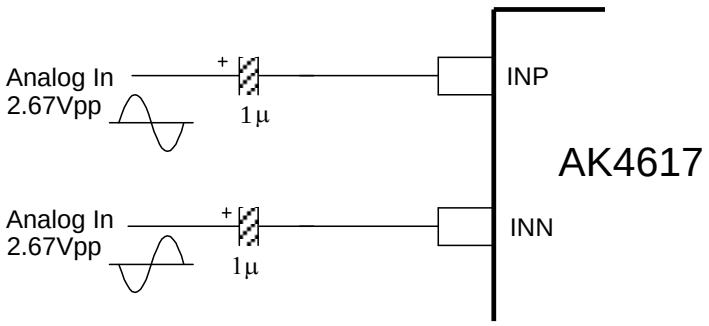


Figure 55. Input Buffer Circuit Example 2 (AC coupled differential input)
(IN1P/IN1N, IN2P/IN2N pins)

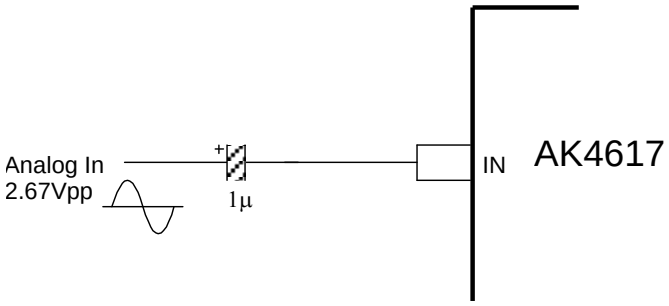


Figure 56. Input Buffer Circuit Example 3 (AC coupled single-ended input)
(IN1, IN2 pins)

■ External Analog Outputs Circuit

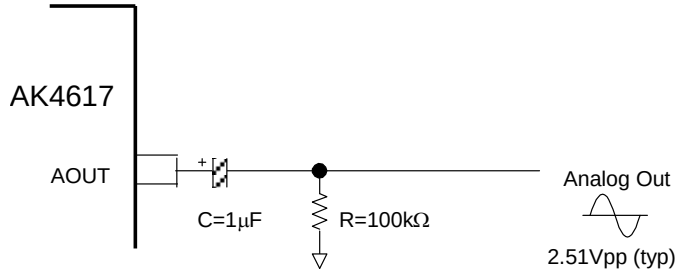


Figure 57. External Circuit Example (LOUT1-6, ROUT1-6 pins)

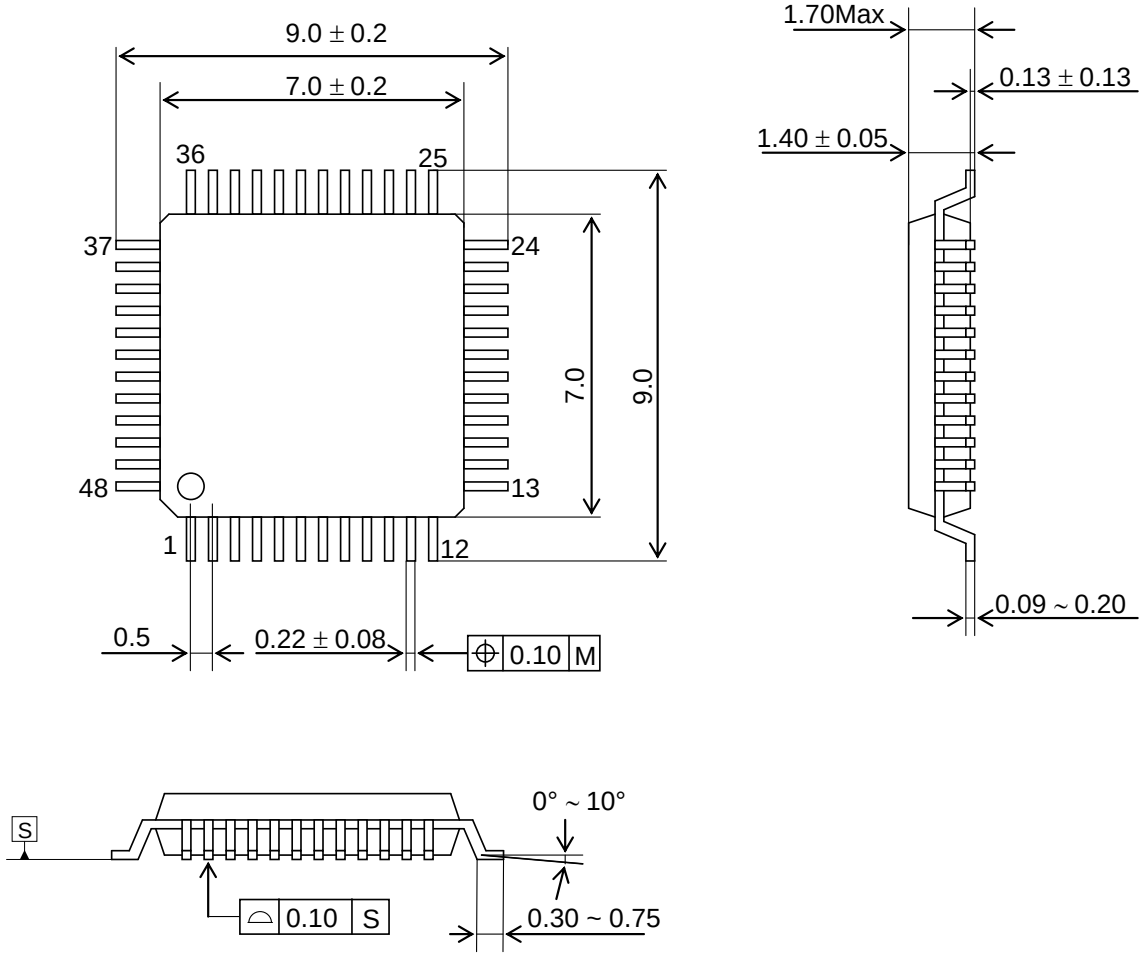
Note: The cut-off frequency (fc) of HPF is determined by following equation.

$$fc = 1/(2 \times \pi \times R \times C)\ [Hz]$$

Where the C is the external AC coupling capacitor and the R is load resistance.
When C = 1μF and R = 100kΩ, then fs = 1.6Hz.

17. Package

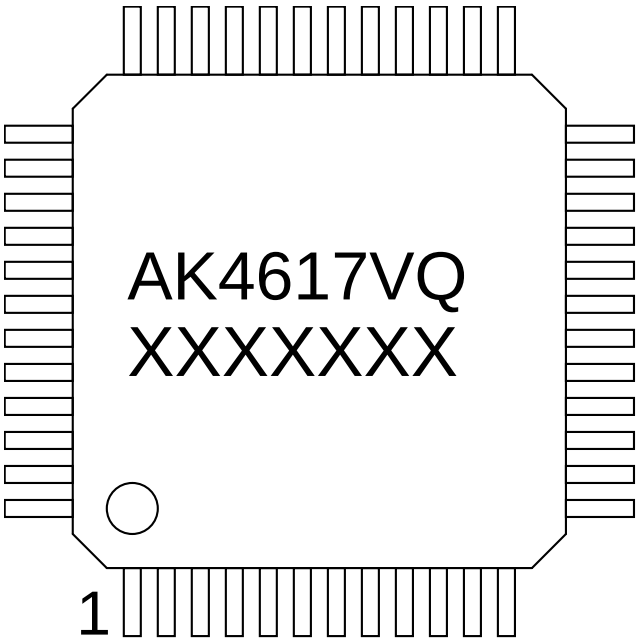
48pin LQFP(Unit: mm)



■ Package & Lead frame material

Package molding compound:	Epoxy resin, Halogen (Br, Cl) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

■ Marking



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4617VQ

18. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
13/11/12	00	First Edition		
14/07/22	01	Error Correction	30	■ Audio Serial Interface Format (2) TDM Mode ADC (four channels) → ADC (two channels)
			42	■ Soft Mute Operation A description about the SMUTEN pin was added. "SMUTEN bit is returned to "0"" → "SMUTEN bit is returned to "1""
			48	■ Serial Control Interface (2) I^2C bus Control Mode "The most significant seven bit" → "The most significant five bits"
			52	■ Register Definitions PMADC: "Power management of mono-stereo" → "Power management of ADC"
			56-58	16. Recommended External Circuits Figure 52-54 were changed.
			59	■ Analog Inputs Description was changed.

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.