

XtremeDSP™ Solution FMC-Video Daughter Board

Technical Reference Guide

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Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|----------|---------|---|
| 10/29/07 | 1.0 | Initial Xilinx release. |
| 02/08/08 | 1.1 | Updated “Files” in Chapter 3. Added note to Table 4-2 . |

Table of Contents

| | |
|--|----|
| Revision History | 2 |
| Figures | 5 |
| Tables | 7 |
| Preface: About This Guide | |
| Guide Contents | 9 |
| Additional Resources | 9 |
| Glossary | 9 |
| Conventions | 10 |
| Typographical | 10 |
| Online Document | 11 |
| Chapter 1: Introduction | |
| Hardware Dependencies | 13 |
| Chapter 2: Hardware Overview | |
| DVI Input | 16 |
| Connector | 16 |
| Analog Interface | 16 |
| Digital Receiver | 16 |
| DDC-EDID | 17 |
| Composite/S-Video Input | 17 |
| Connectors | 17 |
| Video Decoder | 17 |
| Camera Inputs | 17 |
| Connector | 17 |
| Deserializer | 18 |
| Composite/S-Video Output | 18 |
| Connectors | 18 |
| Video Encoder | 18 |
| I2C Buses | 18 |
| FMC I2C | 18 |
| Control I2C | 19 |
| Clocks | 20 |
| Carrier-to-Mezzanine (C2M) Clock | 20 |
| Mezzanine-to-Carrier (M2C) Clock | 20 |
| Power | 21 |
| Signal Bus Multiplexing | 22 |
| DVI Bus Multiplexing | 22 |
| Video Input Multiplexing | 22 |
| FMC Low Pin Count Connector | 22 |

| | |
|----------------------------------|----|
| Standard Pinout | 22 |
| FMC-Video Assigned Signals | 23 |
| LEDs | 26 |
| Mechanical | 26 |

Chapter 3: Tools and Files

| | |
|--------------------|----|
| Design Tools | 27 |
| Files | 27 |

Chapter 4: Test Designs

| | |
|----------------------------------|----|
| Loopback Design | 29 |
| Test Setup | 29 |
| Required Hardware | 29 |
| DVI Loopback | 29 |
| S-Video Loopback | 29 |
| Composite Loopback | 29 |
| Camera Test | 29 |
| Firmware Files | 30 |
| Test Descriptions | 30 |
| DVI-Digital | 31 |
| DVI-Analog | 31 |
| S-Video | 31 |
| Composite | 31 |
| Camera 1 | 31 |
| Camera 2 | 31 |
| Pass-Through Design | 32 |
| Test Setup | 32 |
| Required Hardware | 32 |
| DVI Pass-Through | 32 |
| S-Video Pass-Through | 32 |
| Composite Loopback | 32 |
| Camera Test | 32 |
| Firmware Files | 33 |
| Mode Descriptions | 33 |
| DVI-Digital | 34 |
| DVI-Analog | 34 |
| Camera 1 | 34 |
| Camera 2 | 34 |
| S-Video | 34 |
| Composite | 34 |

Schedule of Figures

Chapter 1: Introduction

Chapter 2: Hardware Overview

| | |
|---|----|
| <i>Figure 2-1: FMC-Video Block Diagram</i> | 15 |
| <i>Figure 2-2: Port Diagram</i> | 16 |
| <i>Figure 2-3: FMC I2C Bus</i> | 19 |
| <i>Figure 2-4: Control I2C Bus</i> | 19 |
| <i>Figure 2-5: Clock Routing</i> | 21 |
| <i>Figure 2-6: Signal Definitions for Low Pin Count Connector</i> | 23 |

Chapter 3: Tools and Files

Chapter 4: Test Designs

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Schedule of Tables

Chapter 1: Introduction

Chapter 2: Hardware Overview

| | |
|--|----|
| <i>Table 2-1: S-Video Port Pinout</i> | 17 |
| <i>Table 2-2: Camera Connector Pinout</i> | 17 |
| <i>Table 2-3: I2C I/O Expander Signal List</i> | 20 |
| <i>Table 2-4: FMC Power Supplies</i> | 21 |
| <i>Table 2-5: FMC-Video Power Supply Voltage Rails</i> | 21 |
| <i>Table 2-6: FMC-Video Assigned Signals</i> | 23 |
| <i>Table 2-7: Board LEDs</i> | 26 |

Chapter 3: Tools and Files

Chapter 4: Test Designs

| | |
|---|----|
| <i>Table 4-1: Firmware Files</i> | 30 |
| <i>Table 4-2: Test Summary</i> | 30 |
| <i>Table 4-3: Firmware Files</i> | 33 |
| <i>Table 4-4: Mode Descriptions</i> | 33 |

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About This Guide

This user guide describes how to use the FMC-Video daughter card, which is a part of the Spartan-3A DSP Video Starter Kit (VSK) for firmware development. The user guide includes descriptions of the hardware, software tools, files, and test designs that are used.

Guide Contents

This manual contains the following chapters:

- [Chapter 1, “Introduction”](#) introduces the FMC-Video daughter card, its interfaces, and hardware dependencies.
- [Chapter 2, “Hardware Overview”](#) discusses each aspect of the FMC-Video daughter board, including its several video interfaces. The board is designed to the VITA-57.1 FMC specification, which includes connectors for power, control, and data.
- [Chapter 3, “Tools and Files”](#) briefly covers the design tools and files that are available.
- [Chapter 4, “Test Designs”](#) describes the Loopback and Pass-through test designs that are used for programming and testing the hardware.

Additional Resources

To find additional documentation, see the Xilinx website at:

<http://www.xilinx.com/literature>.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

<http://www.xilinx.com/support>.

Glossary

The following is a list of terms used in this document:

| | |
|--------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DDC | Data Display Channel |
| DVD | Digital Versatile Disc or Digital Video Disc |
| DVI | Digital Visual Interface |
| EDID | Extended Display Identification Data |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |

| | |
|----------------------|---|
| FMC | FPGA Mezzanine Card Standard (VITA-57.1) |
| FPGA | Field Programmable Gate Array |
| I ² C/I2C | Inter-Integrated Circuit |
| IC | Integrated Circuit |
| LED | Light Emitting Diode |
| LVDS | Low Voltage Differential Signaling |
| MSPS | Mega-Samples Per Second |
| NTSC | National Television System Committee (SDTV broadcast standard originating from U.S.) |
| PAL | Phase Alternating Line (international SDTV broadcast standard) |
| PC | Personal Computer |
| SDTV | Standard Definition Television |
| SECAM | <i>Sequential Couleur Avec Memoire (French) (sequential color with memory)</i> (An international SDTV broadcast standard originating from France) |
| TMDS | Transition Minimized Differential Signaling |
| VITA | VMEbus International Trade Association |
| VGA | Video Graphics Array |
| VSK | Spartan-3A DSP Video Starter Kit |

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

| Convention | Meaning or Use | Example |
|-----------------------|---|------------------------------------|
| Courier font | Messages, prompts, and program files that the system displays | speed grade: - 100 |
| Courier bold | Literal commands that you enter in a syntactical statement | ngdbuild <i>design_name</i> |
| Helvetica bold | Commands that you select from a menu | File → Open |
| | Keyboard shortcuts | Ctrl+C |

| Convention | Meaning or Use | Example |
|-------------------------|---|--|
| Italic font | Variables in a syntax statement for which you must supply values | <code>ngdbuild <i>design_name</i></code> |
| | References to other manuals | See the <i>Development System Reference Guide</i> for more information. |
| | Emphasis in text | If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected. |
| Square brackets [] | An optional entry or parameter. However, in bus specifications, such as <code>bus [7:0]</code> , they are required. | <code>ngdbuild [<i>option_name</i>] <i>design_name</i></code> |
| Braces { } | A list of items from which you must choose one or more | <code>lowpwr = {on off}</code> |
| Vertical bar | Separates items in a list of choices | <code>lowpwr = {on off}</code> |
| Vertical ellipsis . | Repetitive material that has been omitted | IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . . |
| Horizontal ellipsis ... | Repetitive material that has been omitted | <code>allow block <i>block_name</i> loc1 loc2 ... locn;</code> |

Online Document

The following conventions are used in this document:

| Convention | Meaning or Use | Example |
|---------------------------------------|--|---|
| Blue text | Cross-reference link to a location in the current document | See the section “ Additional Resources ” for details. Refer to “ Title Formats ” in Chapter 1 for details. |
| Red text | Cross-reference link to a location in another document | See Figure 2-5 in the <i>Virtex-II Platform FPGA User Guide</i> . |
| Blue, underlined text | Hyperlink to a website (URL) | Go to http://www.xilinx.com for the latest speed files. |

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Introduction

The FMC-Video is a hardware daughter board that includes video interfaces and the circuitry necessary for connection to an FPGA device via a daughter card connector on the carrier board. The carrier/daughter board interface is intended to follow the VITA-57.1 FPGA Mezzanine Card (FMC) standard. This board is part of the Spartan-3A DSP Video Starter Kit (VSK) for firmware development and serves as a hardware reference design.

Hardware Dependencies

The specific carrier platform that is currently validated to support the FMC-Video daughter card is the Spartan-3A DSP FPGA 3400A Development Platform (Part number HW-SD3400A-DSP-DB-UNI-G). See www.xilinx.com for details.

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Hardware Overview

The FMC-Video daughter board (hereafter referred to as FMC -Video) includes several video interfaces. A DVI connector supports both analog and digital video data. SDTV input is supported through S-Video and composite inputs. Two 8P8C modular connectors are included to interface to two cameras. S-Video and composite outputs are also included. FMC-Video includes the necessary circuitry to receive or transmit on each of these interfaces. The board is designed to the VITA-57.1 FMC specification, which includes a connector for power, control, and data. Each aspect of this board is discussed more thoroughly in the following sections.

See [Figure 2-1](#) for the block diagram and [Figure 2-2](#) for the port diagram.

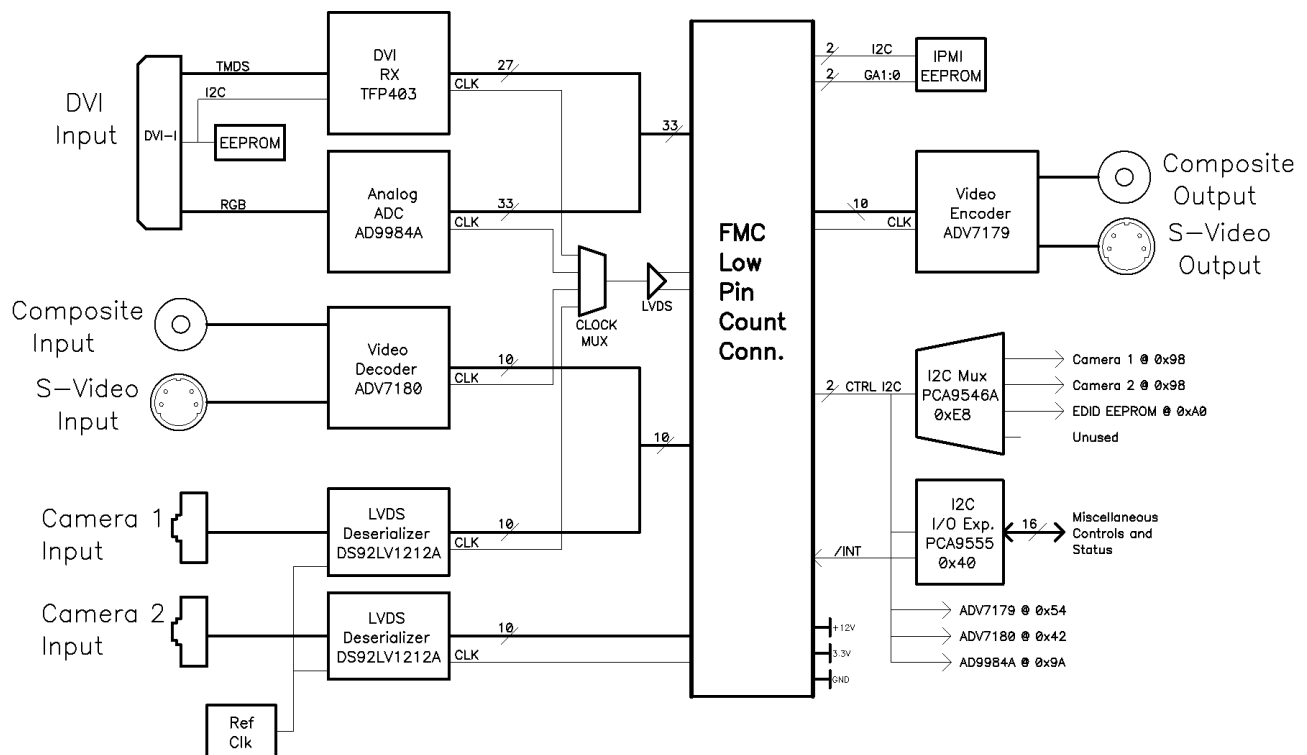


Figure 2-1: FMC-Video Block Diagram

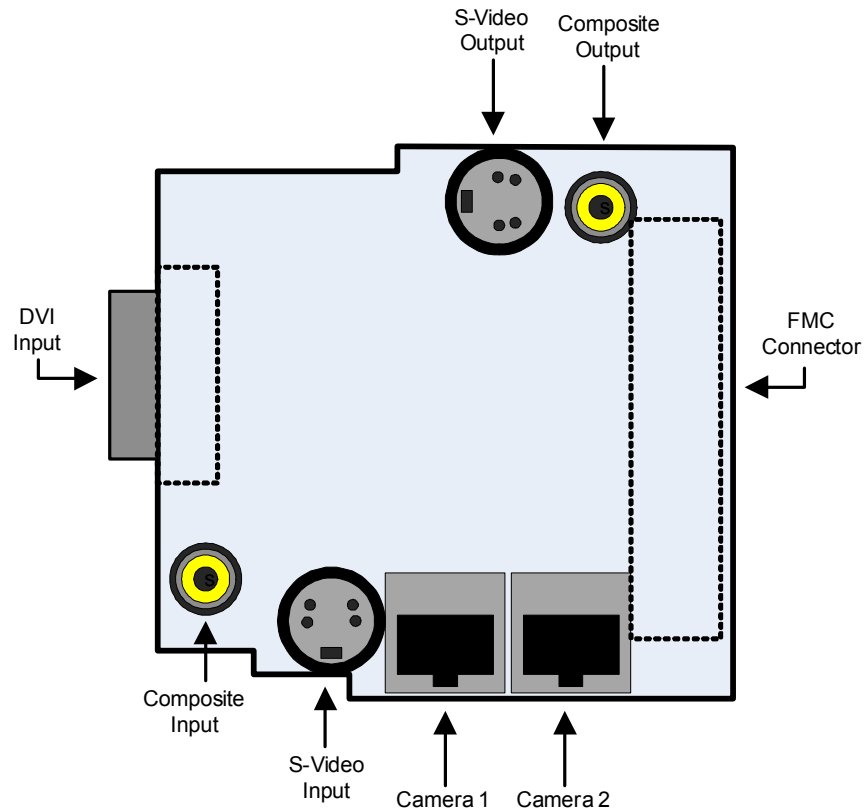


Figure 2-2: Port Diagram

DVI Input

The Digital Visual Interface (DVI) input on this board supports the DVI 1.0 specification for combined single-link digital and analog video.

Connector

The DVI input uses the DVI-I connector to support both digital and analog interfaces.

Analog Interface

The analog interface of the DVI input is implemented through the use of the Analog Devices AD9984A high performance 10-bit display interface IC. This part supports sample rates at up to 170 Mega-Samples Per Second (MSPS) on three 10-bit analog-to-digital converters. The AD9984A includes an on-chip Phase Locked Loop (PLL) to generate a sample clock with complete sync processing. This IC also supports offset and gain adjustments.

Digital Receiver

The Texas Instruments TFP403 DVI receiver IC is used to capture the digital Transition Minimized Differential Signaling (TMDS) signaling used by the digital interface. This part supports the full DVI single-link bandwidth of up to 165 MSPS.

DDC-EDID

The DVI input supports identification through the use of an Extended Display Identification Data (EDID) structure available through the Display Data Channel (DDC) interface. This consists of an I²C EEPROM that is powered through the DVI connector and accessible through the connector. The FMC-Video board also includes the ability to access this EEPROM internally for programming it, as outlined in the “Control I2C” section.

Composite/S-Video Input

Connectors

This video interface is provided via two connectors: a female DIN 4 connector for S-Video and an RCA phone jack for composite signals. The pinout for the S-Video connector is given in [Table 2-1](#). These connectors are industry standard.

Table 2-1: S-Video Port Pinout

| Pin Number | Signal |
|------------|-----------------------|
| 1 | Ground (Y) |
| 2 | Ground (C) |
| 3 | Intensity (Luminance) |
| 4 | Color (Chrominance) |

Video Decoder

The Analog Devices ADV7180 10-bit 4x over-sampling SDTV Video Decoder IC is used to receive and digitize the composite or S-video input. This part can automatically detect and convert standard analog baseband television signals, including National Television System Committee (NTSC), Phase Alternating Line (PAL), and *Sequential Couleur Avec Memoire (Fr.)* (SECAM). The output of this device is 4:2:2 8-bit component video data.

Camera Inputs

FMC-Video includes two camera interfaces to allow the capture of data from two cameras simultaneously. The camera is a custom camera based on a Micron MT9V022 Digital CMOS image sensor.

Connector

The camera interface is based on an RJ45 connector using a proprietary pinout. At the moment the only camera that can be used with this connector is the one that is designed for the Xilinx VSK. The pinout for this connector is given in [Table 2-2](#).

Table 2-2: Camera Connector Pinout

| Pin Number | Signal Name | Direction |
|------------|-------------|-----------|
| 1 | LVDS_P | In |
| 2 | LVDS_N | In |
| 3 | CLK_P | In |

Table 2-2: Camera Connector Pinout (Cont'd)

| Pin Number | Signal Name | Direction |
|------------|-------------|-----------|
| 4 | VCC (5V) | Out |
| 5 | SCL | I/O |
| 6 | CLK_N | In |
| 7 | SDA | I/O |
| 8 | GND | - |

Warning: The RJ45 connectors on FMC-Video are *not* Ethernet ports. Connecting anything other than the camera supplied with VSK to these ports could result in damage to your equipment.

Deserializer

The data stream from the camera is in the form of a high-speed LVDS data stream. This stream is received and deserialized using a National DS92LV1212A deserializer. This is capable of carrying LVDS data from a camera which has a pixel rate of 26.6 MHz.

The deserializer requires a reference clock that is provided via a fixed-frequency 27 MHz oscillator.

Composite/S-Video Output

Connectors

This video interface is provided via two connectors: a female DIN 4 connector for S-Video and an RCA phone jack for composite signals. These connectors are industry standard.

Video Encoder

The Analog Devices ADV7179 PAL/NTSC Video Encoder IC is used to drive the S-Video output. This part is given 8-bit 4:2:2 component video data. The pixel clock frequency is generated by the carrier.

I²C Buses

FMC-Video includes two completely separate I²C buses. One is defined by the FMC specification, the other is for general control of components on the carrier card.

FMC I²C

The FMC specification includes an I²C bus as part of the interface. The mezzanine card is required to include an EEPROM that is read by the carrier card to identify and configure the interface for the mezzanine card. The only device connected to this I²C bus is this EEPROM, which is powered by the 3P3VAUX power supply.

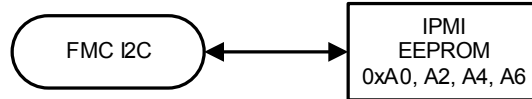
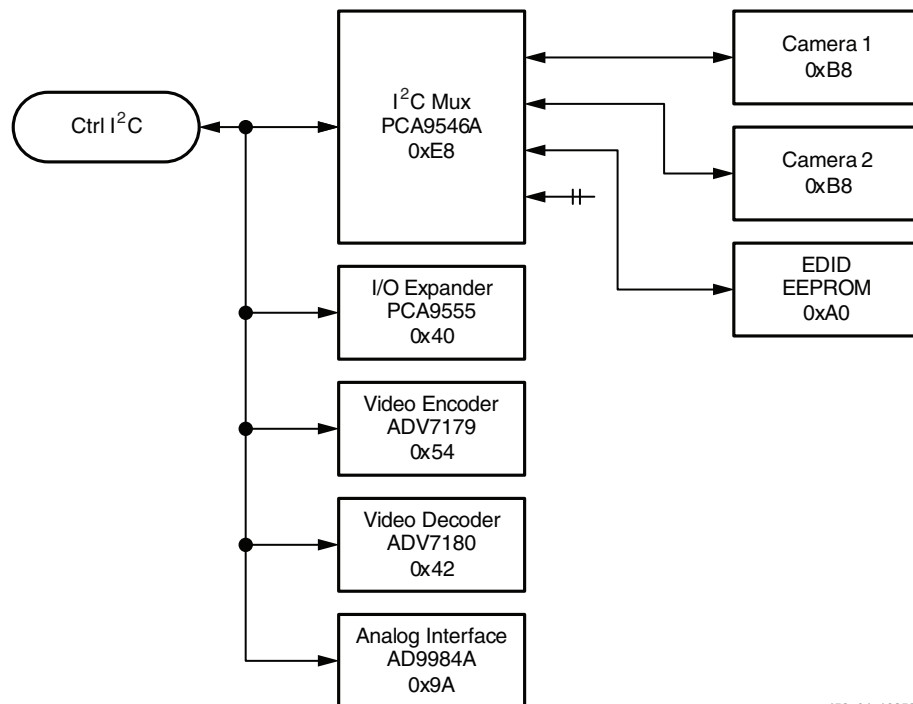


Figure 2-3: FMC I2C Bus

Control I2C

Two of the general-purpose I/O pins of the FMC interface are used to implement an I2C bus to be used for general configuration and status. It was necessary to separate these devices from the FMC I2C bus due to potential I2C device address conflicts that would occur with some of the IC and FMC slot configurations. Separating this bus eliminates this danger.

As shown in Figure 2-4, this I2C bus directly connects to three of the video ICs, an I/O expander, and an I2C mux. The interface to the video IC is used to configure these interfaces. The I2C multiplexer is used to access three other devices. These devices include the two cameras and the EDID EEPROM. The two cameras must be isolated behind this switch because they are at the same device address and would conflict if both connected to the same bus. The EDID EEPROM must be isolated since this bus normally has an I2C master at the DVI video source. The interface to the EDID EEPROM should only be used to program the EEPROM at times when it will not be read by the remote master.



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Figure 2-4: Control I2C Bus

The I/O expander is used to interface to miscellaneous control and status signals, as identified in Table 2-3.

Table 2-3: I²C I/O Expander Signal List

| Signal | Name | Direction | Description |
|--------|--------------|-----------|--|
| P00 | /RESET | O | Reset signal to PCA9546A, ADV7179, ADV7180. |
| P01 | /CAM2_LOCK | I | Lock signal from Camera 2 deserializer. |
| P02 | /CAM2_PD | O | Power down control to Camera 2. |
| P03 | /VIDIN_INT | I | Interrupt signal from ADV7180. |
| P04 | CAM1_OE | O | Output Enable signal to Camera 1 deserializer. |
| P05 | /CAM1_PD | O | Power down control to Camera 1. |
| P06 | /CAM1_LOCK | I | Lock signal from Camera 1 deserializer. |
| P07 | DVIIN_CLKINV | O | Select TFP403 Clock edge |
| P10 | DVI_5V | I | Plug detect signal from DVI connector. |
| P11 | DVIIN_ST | O | Select TFP403 Drive Strength |
| P12 | DVIIN_SCDT | I | Scan detect from DVI digital receiver. |
| P13 | DVIIN_OE | O | Output Enable signal to DVI digital receiver. |
| P14 | CLKMUX_SEL0 | O | Clock Multiplexor select bit 0. |
| P15 | CLKMUX_SEL1 | O | Clock Multiplexor select bit 1. |
| P16 | /PGOOD | I | Power good status from Power Monitor. |
| P17 | /STATUS_LED | O | Software Ready Status LED, low to turn on. |

Clocks

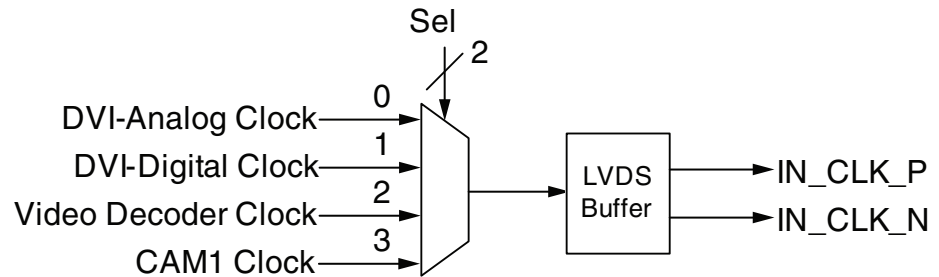
FMC-Video only has one clock input and one clock output from the FMC connector.

Carrier-to-Mezzanine (C2M) Clock

The clock input to FMC-Video is used to drive the video encoder for the S-Video output, typically at 27 MHz.

Mezzanine-to-Carrier (M2C) Clock

This clock output is needed by all of the video interfaces, which includes four sources: DVI-Analog, DVI-Digital, the video decoder, and camera input 1. This requires a clock multiplexor, the ICS83054I. The select lines to this multiplexor are driven by the I²C I/O Expander. The clock multiplexor circuit is diagrammed in [Figure 2-5](#).



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Figure 2-5: Clock Routing

The DVI clocks can be up to 162 MHz, the video decoder clock is 27 MHz, and the camera clock is 26.6 MHz.

To support the second camera input simultaneously, its clock is provided separately on the LA01_P_CC pin.

Power

All power to this board is provided via the FMC connector. There were two available sources for 3.3V, the main 3P3V supply, and VADJ. VADJ must be configured to 3.3V for the 3.3V LVCMOS I/O used for the FMC signal interface. VADJ was chosen to isolate the FMC-Video board from the carrier board 3.3V supply. None of the signals require a reference voltage, so VREF_A_M2C is not required and tied to ground. Table 2-4 outlines the power supply voltages on the low-pin-count FMC connector.

Table 2-4: FMC Power Supplies

| Source | Voltage | Current | Load |
|---------|---------|----------|--------------------------|
| 3P3VAUX | 3.3V | < 1 mA | IPMI EEPROM |
| 3P3V | 3.3V | 0 | Unused |
| VADJ | 3.3V | < 800 mA | 3.3V logic and 1.8V core |
| VREFA | 0V | 0 | Unused. |
| 12P0V | 12.0V | < 128 mA | 5V for Cameras |

Overall current draw for each supply coming from the carrier shall not exceed limits set forth by VITA-57. Test points shall be provided for all power supplies on the board.

Table 2-5 lists the voltage rails present on FMC-Video:

Table 2-5: FMC-Video Power Supply Voltage Rails

| Voltage | Source | Current | Load |
|---------|--------|---------|----------------------------------|
| 1.8V | VADJ | 450 mA | AD9884 and ADV7180 core voltage. |
| 3.3V | VADJ | < 400mA | Miscellaneous ICs, Digital I/O |
| 5.0V | 12P0V | <128 mA | Cameras |

Analog and digital power supplies are isolated using ferrites and proper grounding layout.

Signal Bus Multiplexing

Because of the large number of signals required by each of the video interfaces and the limited number of signals on the FMC connector, it is not possible to dedicate a connector pin for each of the data bits. To fit within the connector signal count, some signals must be shared. Rather than using traditional bus multiplexor ICs, which add cost, board space, and latency to the signals, some of the signals can be multiplexed by sharing nets and controlling the signal output enables. This was done with two pairs of data buses.

DVI Bus Multiplexing

The DVIIN_x signals are shared between the DVI analog interface and the DVI digital receiver. The DVI receiver outputs are high-impedance when the PDO_L pin is asserted Low. This pin is controlled by the DVIIN_OE signal on the I²C I/O expander. The default of this is Low, not enabled. The outputs of the DVI analog interface, the AD9884A, can be disabled through its I²C control registers. Its default state is output enabled. To prevent bus contention, only one of these interfaces can be enabled at a time.

Note: The data width from the analog interface is 10 bits, while the data width from the digital receiver is only 8 bits. This means that two of the bits are not shared. These signals were connected such that the two devices use the same bit as the most significant bit, bit 9. The digital receiver does not use bits 1 and 0.

Video Input Multiplexing

The VIDIN_x signals are shared between the video decoder and camera 1. The camera 1 signals are set to high impedance using the REN pin on the deserializer, driven by the net CAM1_OE, from the I²C I/O expander. The default state is Low, not enabled. The outputs of the video decoder, the ADV7180, are disabled through its I²C control registers. The default state is enabled. To prevent bus contention only one of these interfaces can be enabled at a time.

FMC Low Pin Count Connector

Standard Pinout

The VITA-57 FMC connector is of the low-pin-count (LPC) variant. All I/O on this connector shall be 3.3V single ended, with the exception of two LVDS clocks. The available pins in the LPC connector are in rows C, D, G, and H, as shown in [Figure 2-6](#).

| | K | J | H | G | F | E | D | C | B | A |
|----|----|----|-------------|------------|----|----|---------------|-----------|----|----|
| 1 | NC | NC | VREF_A M2C | GND | NC | NC | PG_C2M | GND | NC | NC |
| 2 | NC | NC | PRSNT_M2C_L | CLK0_C2M_P | NC | NC | GND | DP0_C2M_P | NC | NC |
| 3 | NC | NC | GND | CLK0_C2M_N | NC | NC | GND | DP0_C2M_N | NC | NC |
| 4 | NC | NC | CLK0_M2C_P | GND | NC | NC | GBTCLK0_M2C_P | GND | NC | NC |
| 5 | NC | NC | CLK0_M2C_N | GND | NC | NC | GBTCLK0_M2C_N | GND | NC | NC |
| 6 | NC | NC | GND | LA00_P_CC | NC | NC | GND | DP0_M2C_P | NC | NC |
| 7 | NC | NC | LA02_P | LA00_N_CC | NC | NC | GND | DP0_M2C_N | NC | NC |
| 8 | NC | NC | LA02_N | GND | NC | NC | LA01_P_CC | GND | NC | NC |
| 9 | NC | NC | GND | LA03_P | NC | NC | LA01_N_CC | GND | NC | NC |
| 10 | NC | NC | LA04_P | LA03_N | NC | NC | GND | LA06_P | NC | NC |
| 11 | NC | NC | LA04_N | GND | NC | NC | LA05_P | LA06_N | NC | NC |
| 12 | NC | NC | GND | LA08_P | NC | NC | LA05_N | GND | NC | NC |
| 13 | NC | NC | LA07_P | LA08_N | NC | NC | GND | GND | NC | NC |
| 14 | NC | NC | LA07_N | GND | NC | NC | LA09_P | LA10_P | NC | NC |
| 15 | NC | NC | GND | LA12_P | NC | NC | LA09_N | LA10_N | NC | NC |
| 16 | NC | NC | LA11_P | LA12_N | NC | NC | GND | GND | NC | NC |
| 17 | NC | NC | LA11_N | GND | NC | NC | LA13_P | GND | NC | NC |
| 18 | NC | NC | GND | LA16_P | NC | NC | LA13_N | LA14_P | NC | NC |
| 19 | NC | NC | LA15_P | LA16_N | NC | NC | GND | LA14_N | NC | NC |
| 20 | NC | NC | LA15_N | GND | NC | NC | LA17_P_CC | GND | nc | NC |
| 21 | NC | NC | GND | LA20_P | NC | NC | LA17_N_CC | GND | nc | NC |
| 22 | NC | NC | LA19_P | LA20_N | NC | NC | GND | LA18_P_CC | NC | NC |
| 23 | NC | NC | LA19_N | GND | NC | NC | LA23_P | LA18_N_CC | NC | NC |
| 24 | NC | NC | GND | LA22_P | NC | NC | LA23_N | GND | NC | NC |
| 25 | NC | NC | LA21_P | LA22_N | NC | NC | GND | GND | NC | NC |
| 26 | NC | NC | LA21_N | GND | NC | NC | LA26_P | LA27_P | NC | NC |
| 27 | NC | NC | GND | LA25_P | NC | NC | LA26_N | LA27_N | NC | NC |
| 28 | NC | NC | LA24_P | LA25_N | NC | NC | GND | GND | NC | NC |
| 29 | NC | NC | LA24_N | GND | NC | NC | TCK | GND | NC | NC |
| 30 | NC | NC | GND | LA29_P | NC | NC | TDI | SCL | NC | NC |
| 31 | NC | NC | LA28_P | LA29_N | NC | NC | TDO | SDA | NC | NC |
| 32 | NC | NC | LA28_N | GND | NC | NC | 3P3VAUX | GND | NC | NC |
| 33 | NC | NC | GND | LA31_P | NC | NC | TMS | GND | NC | NC |
| 34 | NC | NC | LA30_P | LA31_N | NC | NC | TRST_L | GA0 | NC | NC |
| 35 | NC | NC | LA30_N | GND | NC | NC | GA1 | 12P0V | NC | NC |
| 36 | NC | NC | GND | LA33_P | NC | NC | 3P3V | GND | NC | NC |
| 37 | NC | NC | LA32_P | LA33_N | NC | NC | GND | 12P0V | NC | NC |
| 38 | NC | NC | LA32_N | GND | NC | NC | 3P3V | GND | NC | NC |
| 39 | NC | NC | GND | VADJ | NC | NC | GND | 3P3V | NC | NC |
| 40 | NC | NC | VADJ | GND | NC | NC | 3P3V | GND | NC | NC |

LPC Connector
LPC Connector
LPC Connector
LPC Connector

Figure 2-6: Signal Definitions for Low Pin Count Connector

FMC-Video Assigned Signals

Table 2-6 lists the FMC-Video assigned signals and their descriptions..

Table 2-6: FMC-Video Assigned Signals

| Net Name | FMC-LPC Signal | Direction | Description |
|--------------|----------------|-----------|---|
| CTRL_SCL | LA18_P_CC | C2M | Control I ² C bus clock |
| CTRL_SDA | LA18_N_CC | bidir | Control I ² C bus data |
| /IOEXP_INT | LA26_N | M2C | I/O expander change interrupt line |
| INCLK_P | CLK0_M2C_P | M2C | Selected Video Input Clock, LVDS+ |
| INCLK_N | CLK0_M2C_N | M2C | Selected Video Input Clock, LVDS- |
| DVIIN_HS | LA22_N | M2C | DVI input HSYNC |
| DVIIN_VS | LA26_P | M2C | DVI input VSYNC |
| DVIIN_DE/FLD | LA22_P | M2C | DVI input Data Enable or Odd/Even Field |
| DVIIN_R9 | LA05_N | M2C | DVI input most significant red data bit |
| DVIIN_R8 | LA10_P | M2C | DVI input red data bit |
| DVIIN_R7 | LA07_N | M2C | DVI input red data bit |
| DVIIN_R6 | LA09_P | M2C | DVI input red data bit |

Table 2-6: FMC-Video Assigned Signals (Cont'd)

| Net Name | FMC-LPC Signal | Direction | Description |
|--------------|----------------|-----------|---|
| DVIIN_R5 | LA10_N | M2C | DVI input red data bit |
| DVIIN_R4 | LA12_P | M2C | DVI input red data bit |
| DVIIN_R3 | LA09_N | M2C | DVI input red data bit |
| DVIIN_R2 | LA13_P | M2C | DVI input red data bit |
| DVIIN_R1 | LA07_P | M2C | DVI input red data bit, 0 & 1 unused for digital mode |
| DVIIN_R0 | LA06_N | M2C | DVI input least significant red data bit |
| DVIIN_G9 | LA05_P | M2C | DVI input most significant green data bit |
| DVIIN_G8 | LA06_P | M2C | DVI input green data bit |
| DVIIN_G7 | LA11_P | M2C | DVI input green data bit |
| DVIIN_G6 | LA12_N | M2C | DVI input green data bit |
| DVIIN_G5 | LA11_N | M2C | DVI input green data bit |
| DVIIN_G4 | LA13_N | M2C | DVI input green data bit |
| DVIIN_G3 | LA16_P | M2C | DVI input green data bit |
| DVIIN_G2 | LA16_N | M2C | DVI input green data bit |
| DVIIN_G1 | LA04_N | M2C | DVI input green data bit, 0 & 1 unused for digital mode |
| DVIIN_G0 | LA04_P | M2C | DVI input least significant green data bit |
| DVIIN_B9 | LA15_P | M2C | DVI input most significant blue data bit |
| DVIIN_B8 | LA17_P_CC | M2C | DVI input blue data bit |
| DVIIN_B7 | LA15_N | M2C | DVI input blue data bit |
| DVIIN_B6 | LA17_N_CC | M2C | DVI input blue data bit |
| DVIIN_B5 | LA20_P | M2C | DVI input blue data bit |
| DVIIN_B4 | LA23_P | M2C | DVI input blue data bit |
| DVIIN_B3 | LA20_N | M2C | DVI input blue data bit |
| DVIIN_B2 | LA23_N | M2C | DVI input blue data bit |
| DVIIN_B1 | LA02_N | M2C | DVI input blue data bit, 0 & 1 unused for digital mode |
| DVIIN_B0 | LA02_P | M2C | DVI input least significant blue data bit |
| VIDIN_HS | LA21_N | M2C | Video input HSYNC or CAM1 Line |
| VIDIN_FLD/VS | LA21_P | M2C | Video input FIELD/VSYNC or CAM1 Frame |
| VIDIN_D7 | LA27_P | M2C | Video input most significant data bit |
| VIDIN_D6 | LA27_N | M2C | Video input data bit |

Table 2-6: FMC-Video Assigned Signals (Cont'd)

| Net Name | FMC-LPC Signal | Direction | Description |
|-----------------|-----------------------|------------------|---|
| VIDIN_D5 | LA25_P | M2C | Video input data bit |
| VIDIN_D4 | LA25_N | M2C | Video input data bit |
| VIDIN_D3 | LA24_P | M2C | Video input data bit |
| VIDIN_D2 | LA24_N | M2C | Video input data bit |
| VIDIN_D1 | LA29_P | M2C | Video input data bit |
| VIDIN_D0 | LA29_N | M2C | Video input least significant data bit |
| CAM2_CLK | LA01_P_CC | M2C | Camera 2 Input Clock |
| CAM2_LINE | LA32_P | M2C | Camera 2 LINE |
| CAM2_FRAME | LA32_N | M2C | Camera 2 Frame |
| CAM2_D7 | LA33_N | M2C | Camera 2 most significant data bit |
| CAM2_D6 | LA33_P | M2C | Camera 2 data bit |
| CAM2_D5 | LA30_N | M2C | Camera 2 data bit |
| CAM2_D4 | LA30_P | M2C | Camera 2 data bit |
| CAM2_D3 | LA31_N | M2C | Camera 2 data bit |
| CAM2_D2 | LA31_P | M2C | Camera 2 data bit |
| CAM2_D1 | LA28_P | M2C | Camera 2 data bit |
| CAM2_D0 | LA28_N | M2C | Camera 2 least significant data bit |
| VIDOUT_CLK | CLK0_C2M_P | C2M | Video Output Clock |
| VIDOUT_HS | LA19_N | M2C | Video output HSYNC |
| VIDOUT_FLD/VS | LA19_P | M2C | Video output FIELD/VSYNC |
| VIDOUT_D7 | LA14_N | M2C | Video output most significant data bit |
| VIDOUT_D6 | LA14_P | M2C | Video output data bit |
| VIDOUT_D5 | LA08_N | M2C | Video output data bit |
| VIDOUT_D4 | LA08_P | M2C | Video output data bit |
| VIDOUT_D3 | LA03_N | M2C | Video output data bit |
| VIDOUT_D2 | LA03_P | M2C | Video output data bit |
| VIDOUT_D1 | LA00_N_CC | M2C | Video output data bit |
| VIDOUT_D0 | LA00_P_CC | M2C | Video output least significant data bit |

LEDs

FMC-Video includes two status LEDs, placed on the back of the board. These LEDs indicate that the board is being powered correctly and the software has initialized it, respectively. See [Table 2-7](#).

Table 2-7: Board LEDs

| Net Name | FMC-LPC Signal | Direction |
|----------|-------------------------------|--------------------------------------|
| 1 | PG | Power supplies are within regulation |
| 2 | I ² C I/O Expander | Software initialization complete |

Mechanical

Wherever possible this module conforms to VITA-57 from a mechanical standpoint. It is impossible to meet the mechanical specs due to the size of the connectors that must be on the board. For instance, all the connectors cannot fit within the I/O envelope height of 9.5 mm on the front of the board. Due to this, some connectors must be put on the back of the board. However, the orientation of these connectors should still support two FMC modules installed side by side on a carrier. To this end, all connectors are oriented toward the front panel side of the board or directly vertical.

Although the mechanical spec is broken by this design, it is possible for mechanical conformance to be achieved by simply removing the connectors that are placed on the back.

Rule 25 of the VITA-57 spec requires a minimum of 500 VDC and 1 MΩ of isolation. The only S-video connectors available for this application are rated at 250 VDC isolation and, therefore, violate this rule. Even with these connectors removed, there is still only 250 VDC isolation, because the spacing between pads on the PCB artwork to accommodate this connector.

Tools and Files

Design Tools

Gerber files were generated from PCAD and PDF files were published for archival purposes and for general viewing.

Files

The current revision of the design references the following files:

| Filename | Revision | Software | Description |
|---------------------------|----------|---------------|-------------------------|
| FMCVIDEOD_gerber.zip | D | Gerber viewer | Gerber files |
| FMCVIDEO_Sch_RevD.pdf | D | Acrobat 7.0 | Schematic in PDF format |
| FMCVIDEO_BOM_AVL_RevD.xls | D | Excel 2003 | Bill of Materials |

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Test Designs

This chapter covers the designs that are used for programming and testing the hardware.

Loopback Design

This is an FPGA design for an FMC-Carrier board that tests the FMC-Video board interfaces by generating test patterns on outputs and testing them on inputs. This test uses a DVI digital and analog output on the carrier board as a test source.

Test Setup

Required Hardware

- FMC-Video installed on a Spartan-3A DSP FPGA 3400A Development Platform
- DVI-I Cable (analog and digital)
- S-Video Cable
- Composite Cable (RCA)
- Two Cameras, MT9V022
- Two Cat-6 cables with 8P8C modular connectors

DVI Loopback

The DVI-I cable connects the DVI output on the carrier board to the DVI input on FMC-Video.

S-Video Loopback

The S-Video cable connects the S-Video output on FMC-Video to the S-Video input on FMC-Video.

Composite Loopback

The composite (RCA) cable connects the Composite output on FMC-Video to the Composite input on FMC-Video.

Camera Test

The camera test is not a loopback. Instead, a camera is connected to each camera port using a Cat-6 cable.

Firmware Files

Table 4-1 lists the firmware files, type, and descriptions.

Note: The PicoBlaze™ code for this design was developed using the pBlaze IDE version 3.6. For details, visit www.mediatronix.com/tools/.

Table 4-1: Firmware Files

| Filename | Type | Description |
|------------------------|-------------|---|
| MDSP_FMCVIDEO_LPBK.v | Verilog | Top Level wrapper for project |
| FMCVIDEO_LPBK_CTRL.v | Verilog | Controller module, including PicoBlaze |
| PB_FMCVIDEO_LPBK.v | Verilog | PicoBlaze Instruction ROM |
| KCPSM3.v | Verilog | PicoBlaze processor |
| VGA_TP_GEN.v | Verilog | VGA test pattern generator |
| CH7301_OUT.v | Verilog | Interface to DVI output |
| DVI_IN.v | Verilog | DVI input module |
| IMAGE_CROP.v | Verilog | Image crop module |
| VGA_TP_TEST.v | Verilog | VGA test pattern comparison module |
| FREQ_COMPARE.v | Verilog | Frequency comparison Module |
| YCrCb422_TP_GEN.v | Verilog | NTSC test pattern generator |
| YCrCb422_TP_TEST.v | Verilog | NTSC test pattern comparison module |
| CAM_TP_TEST.v | Verilog | MT9V022 camera test pattern comparison |
| MDSP_FMCVIDEO_LPBK.ucf | Constraints | Pin and Timing Constraints for Project |
| FMCVIDEO_LPBK.psm | PicoBlaze | PicoBlaze Processor Code |
| helpers.inc | PicoBlaze | Helpful Equates for PicoBlaze Code |
| PB_CODE_template.v | Verilog | Used by pBlazeIDE to generate PB_x.v file |

Test Descriptions

All tests are selected via DIP switches on the carrier board, and errors are indicated via LEDs on the carrier board. See Table 4-2.

Table 4-2: Test Summary

| SW[3:0] | Name | LED[7] | LED[6] | LED[5] | LED[4] |
|---------|------------------|-----------|------------|-------------|------------|
| 0000 | DVI-Digital Test | CLK Error | Red Error | Green Error | Blue Error |
| 0001 | DVI-Analog Test | CLK Error | Red Error | Green Error | Blue Error |
| 0010 | S-Video Test | CLK Error | Data Error | Off | Off |
| 0011 | Composite Test | CLK Error | Data Error | Off | Off |
| 0100 | Camera 1 Test | CLK Error | Data Error | Off | Off |
| 0101 | Camera 2 Test | CLK Error | Data Error | Off | Off |

Notes:

- LED[3:0] display the setting of DIP SW[3:0].

DVI-Digital

The DVI output on the carrier board generates a VGA test pattern of red, green, and blue ramps. This is received by FMC-Video and is compared against what was sent. To pass this test, the received clock frequency must be correct and the test pattern must be received with no errors.

DVI-Analog

The DVI output on the carrier board generates a VGA test pattern of red, green, and blue ramps. This is received by FMC-Video and is compared against what was sent. To pass this test, the received clock frequency must be correct and the test pattern must closely match the test pattern. Since this is an analog interface, the digitized version will never perfectly match the sent image, so some error is acceptable. To pass, the majority of the pixels must be within a small error range of the test pattern value.

S-Video

The S-Video output on the carrier board generates an NTSC test pattern of red, green, and blue ramps. This is received by FMC-Video and is compared against what was sent. To pass this test, the received clock frequency must be correct and the test pattern must closely match the test pattern. Since this is an analog interface, the digitized version will never perfectly match the sent image, so some error is acceptable. To pass, the majority of the pixels must be within a small error range of the test pattern value.

Composite

The composite output on the carrier board generates an NTSC test pattern of red, green, and blue ramps. This is received by FMC-Video and is compared against what was sent. To pass this test, the received clock frequency must be correct and the test pattern must closely match the test pattern. Since this is an analog interface, the digitized version will never perfectly match the sent image, so some error is acceptable. To pass, the majority of the pixels must be within a small error range of the test pattern value.

Camera 1

The camera is configured to generate a test pattern. This is received by FMC-Video and is compared against what the test pattern is supposed to be. To pass this test, the received clock frequency must be correct and the test pattern must be received with no errors.

Camera 2

This test is the same as Camera 1.

Pass-Through Design

This is an FPGA design for an FMC-Carrier board that tests the FMC-Video board interfaces by passing video data through the carrier board FPGA. This test uses a DVI digital and analog output on the carrier board as an output.

Test Setup

Required Hardware

- FMC-Video installed on Spartan-3A DSP FPGA 3400A Development Platform
- Composite/S-Video source (for example, DVD player)
- Composite/S-Video display (for example, TV)
- DVI-I source (for example, PC)
- DVI-I display (for example, LCD computer monitor)
- Two DVI-I Cables (analog and digital)
- Two S-Video Cables
- Two Composite Cables (RCA)
- Two Cameras, MT9V022
- Two Cat-6 cables with 8P8C modular connectors

DVI Pass-Through

One DVI-I cable connects the DVI output on the carrier board to the DVI-I display. The other DVI-I cable connects the DVI output of the DVI-I video source to the DVI input on FMC-Video.

S-Video Pass-Through

One S-Video cable connects the S-Video output on FMC-Video to the S-Video input on the Composite/S-Video display. The other S-Video cable connects the S-Video output on the Composite/S-Video source to the S-Video input on FMC-Video.

Composite Loopback

One composite (RCA) cable connects the composite output on FMC-Video to the composite input on the Composite/S-Video display. The second composite cable connects the composite output on the Composite/S-Video source to the composite input on FMC-Video.

Camera Test

One camera is connected to each camera port using a Cat-6 cable.

Firmware Files

Table 4-3 lists the firmware files, type, and descriptions.

Note: The PicoBlaze code for this design was developed using the pBlaze IDE version 3.6. For details, visit <http://www.mediatronix.com/tools/>.

Table 4-3: **Firmware Files**

| Filename | Type | Description |
|--------------------------|-------------|---|
| MDSP_FMCVIDEO_PASS.v | Verilog | Top Level wrapper for project |
| FMCVIDEO_PASS_CTRL.v | Verilog | Controller module, including PicoBlaze |
| PB_FMCVIDEO_PASS.v | Verilog | PicoBlaze Instruction ROM |
| KCPSM3.v | Verilog | PicoBlaze processor |
| DVI_IN.v | Verilog | DVI input module |
| IMAGE_CROP.v | Verilog | Image crop module |
| YCrCb422_IN.v | Verilog | Video input module |
| MICRON_IMAGE_SENSOR_IN.v | Verilog | Micron Image Sensor Input module |
| YCrCb422_OUT.v | Verilog | Video Output Module |
| CH7301_OUT.v | Verilog | Interface to DVI output |
| MDSP_FMCVIDEO_PASS.ucf | Constraints | Pin and Timing Constraints for Project |
| FMCVIDEO_PASS.psm | PicoBlaze | PicoBlaze Processor Code |
| helpers.inc | PicoBlaze | Helpful Equates for PicoBlaze Code |
| PB_CODE_template.v | Verilog | Used by pBlazeIDE to generate PB_x.v file |

Mode Descriptions

All modes are selected via DIP switches on the carrier board. See Table 4-4

Table 4-4: **Mode Descriptions**

| SW[3:0] | Name | Input | Output |
|---------|---------------------|-------------|----------------------|
| 0000 | DVI-Digital <65 MHz | DVI Digital | DVI Digital & Analog |
| 0001 | DVI-Digital >65 MHz | DVI Digital | DVI Digital & Analog |
| 0010 | DVI-Analog VGA60 | DVI Analog | DVI Digital & Analog |
| 0011 | DVI-Analog SVGA60 | DVI Analog | DVI Digital & Analog |
| 0100 | DVI-Analog XGA60 | DVI Analog | DVI Digital & Analog |
| 0101 | DVI-Analog SXGA60 | DVI Analog | DVI Digital & Analog |
| 0110 | DVI-Analog UXGA60 | DVI Analog | DVI Digital & Analog |
| 1000 | Camera 1 | Camera 1 | DVI Digital & Analog |
| 1001 | Camera 2 | Camera 2 | DVI Digital & Analog |

Table 4-4: Mode Descriptions (Cont'd)

| SW[3:0] | Name | Input | Output |
|---------|-----------|-----------|-----------------------|
| 1010 | S-Video | S-Video | S-Video and Composite |
| 1011 | Composite | Composite | S-Video and Composite |

DVI-Digital

Modes 0 and 1 are both DVI-Digital input. The division at 65 MHz is required by the DVI output on the Carrier board. The captured data is output on the DVI output as both digital and analog.

DVI-Analog

Modes 2 through 6 are analog input. Each analog input resolution requires specific timing and crop settings. The captured data is output on the DVI output as both digital and analog.

Camera 1

The camera is configured and the data is captured by FMC-Video. The captured data is output on the DVI output as both digital and analog.

Camera 2

The camera is configured and the data is captured by FMC-Video. The captured data is output on the DVI output as both digital and analog.

S-Video

The Video decoder is configured to receive S-Video. This is passed to the video encoder and output as both S-Video and Composite.

Composite

The Video decoder is configured to receive Composite Video. This is passed to the video encoder and output as both S-Video and Composite.