
Sup/IRBuck™

USER GUIDE FOR IR3856 EVALUATION BOARD

DESCRIPTION

The IR3856 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 4mmx5mm Power QFN package.

Key features offered by the IR3856 include programmable soft-start ramp, precision 0.7V reference voltage, Power Good, thermal protection, over voltage protection, programmable switching frequency, synchronization to external clock, Sequence input, Enable input, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3856 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3856 is available in the IR3856 data sheet.

BOARD FEATURES

- $V_{in} = +12V$ (13.2V Max)
- $V_{cc} = +5V$ (5.5V Max)
- $V_{out} = +1.8V @ 0- 6A$
- $F_s = 600kHz$
- $L = 1.0uH$
- $C_{in} = 3x10uF$ (ceramic 1206) + 330uF (electrolytic)
- $C_{out} = 4x22uF$ (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 6A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3856 has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). Separate supplies should be applied to these inputs. Vcc input should be a well regulated 4.5V-5.5V supply and it would be connected to Vcc+ and Vcc-.

If single 12V application is required connect R7 (zero Ohm resistor) which enables the on board bias regulator (see schematic). In this case there is no need of external Vcc supply.

The output can track a sequencing input at the start-up. *For sequencing application, R16 should be removed and the external sequencing source should be applied between Seq. and Agnd.* The value of R14 and R28 can be selected to provide the desired ratio between the output voltage and the tracking input. *For proper operation of IR3856, the voltage at Seq. pin should not exceed Vcc.*

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
Vcc+	Vcc input
Vcc-	Ground for Vcc input
VOUT-	Ground of V_{out}
VOUT+	V_{out} (+1.8V)
Enable	Enable
Seq.	Sequence Input
PGood	Power Good Signal
SYNC	External Synchronization Clock

LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. The IR3856 SupIRBuck and all of the passive components are mounted on the top side of the board.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3856. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the SupIRBuck. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

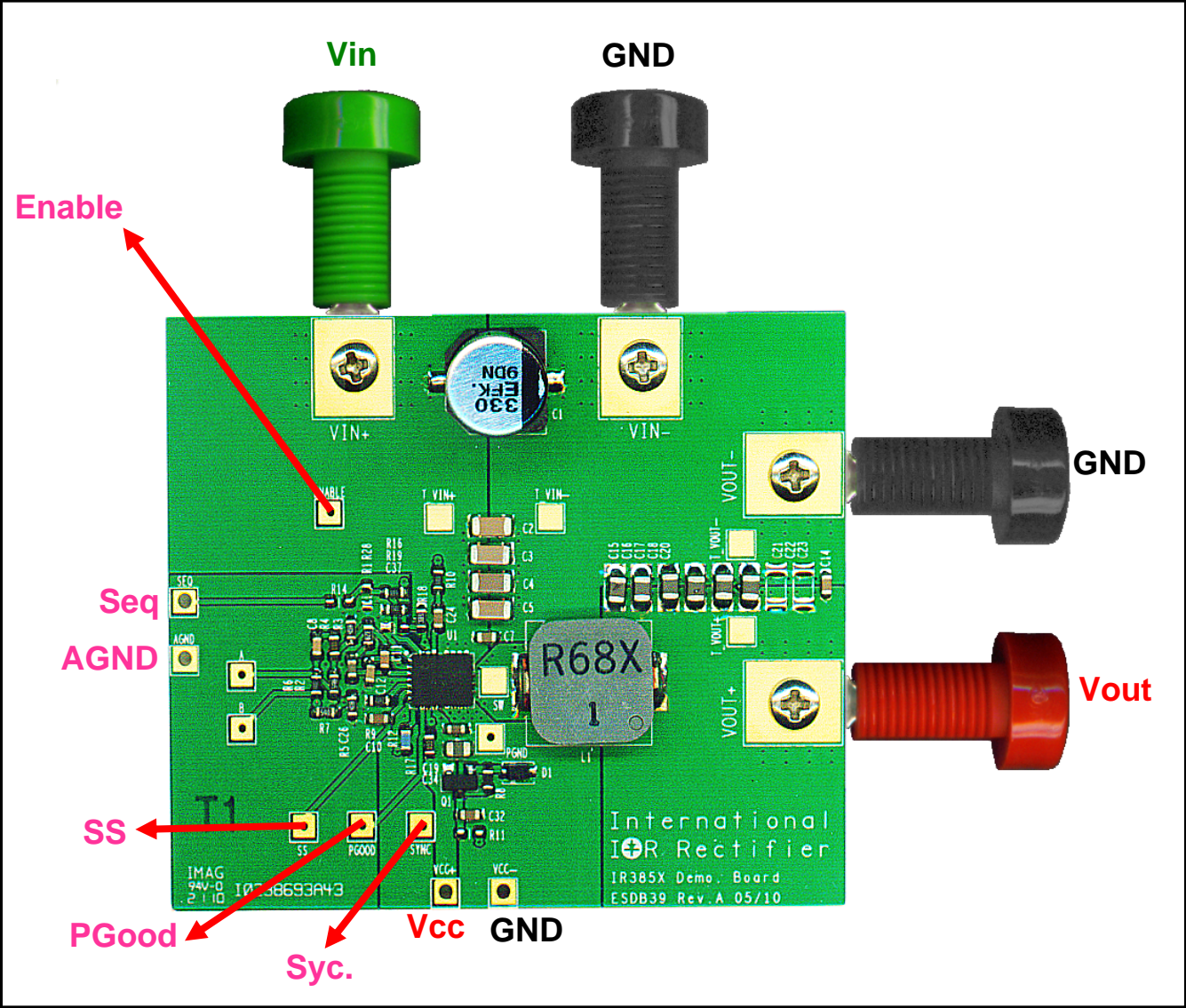


Fig. 1: Connection diagram of IR385x evaluation boards

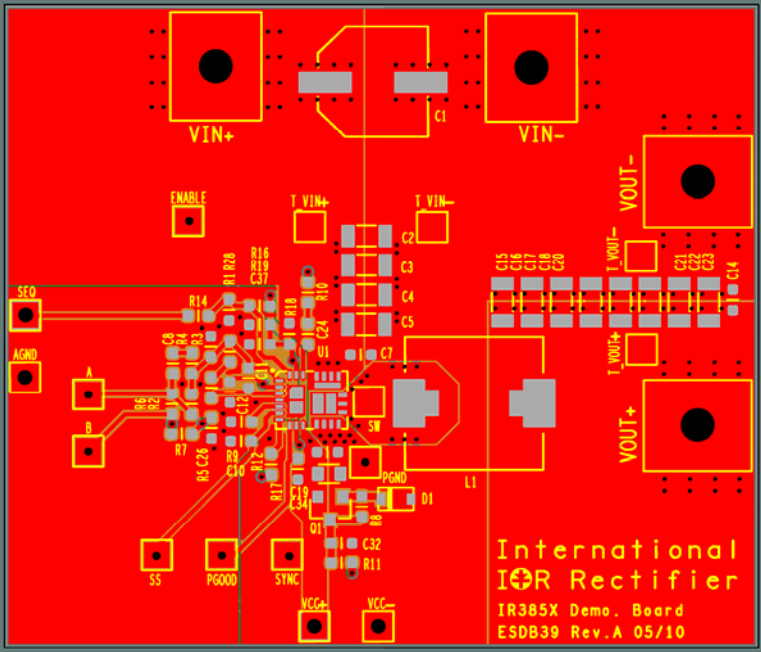


Fig. 2: Board layout, top overlay

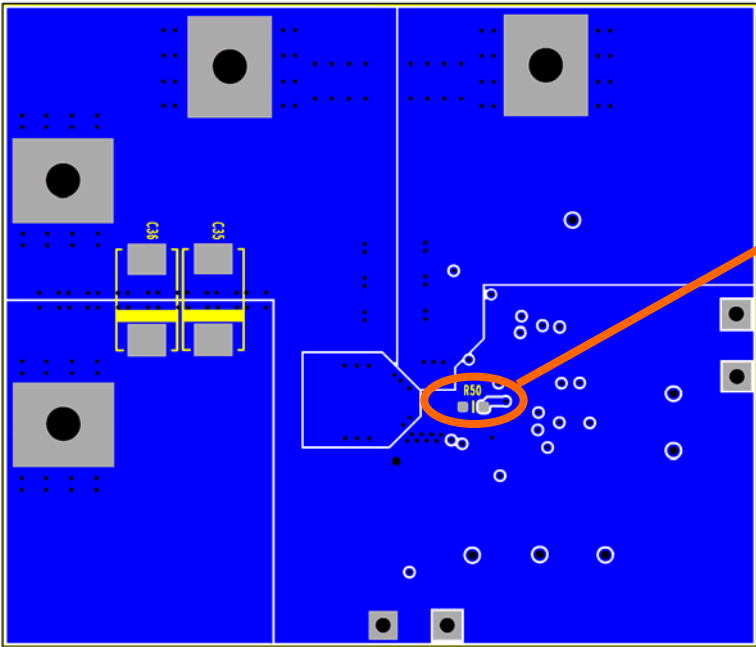


Fig. 3: Board layout, bottom overlay (rear view)

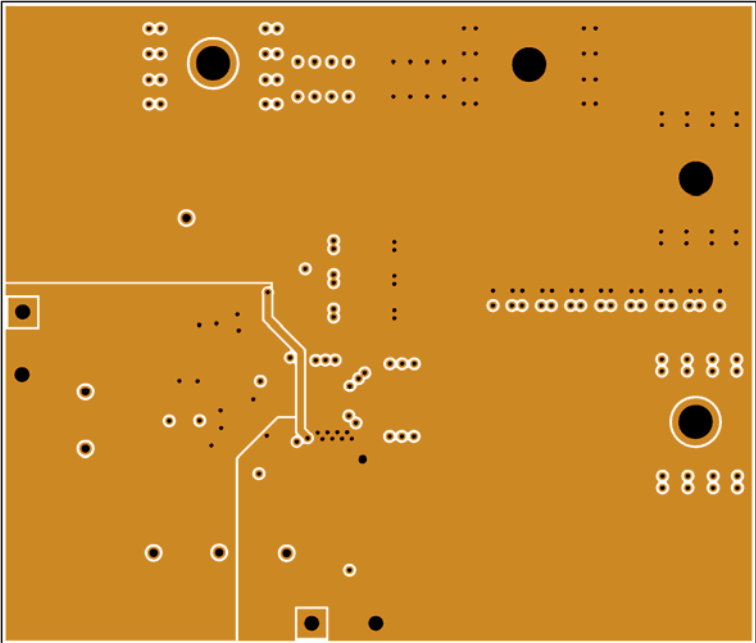


Fig. 4: Board layout, mid-layer I.

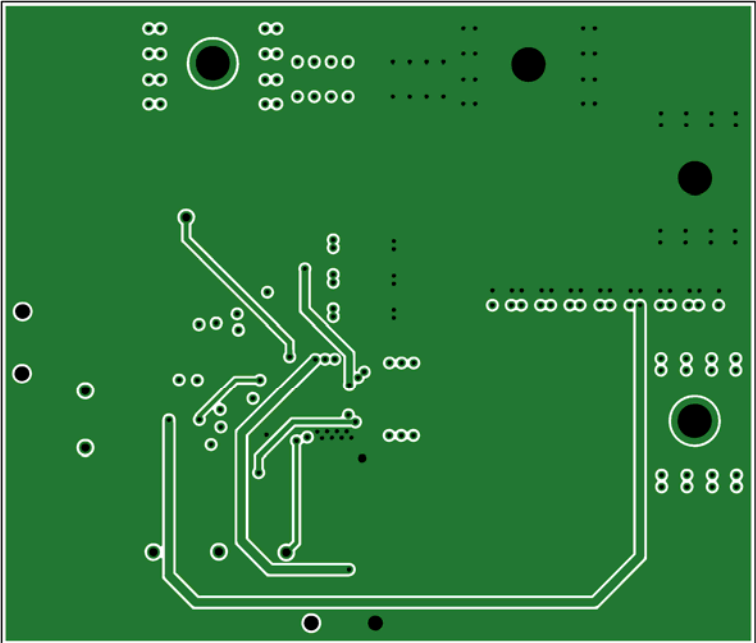
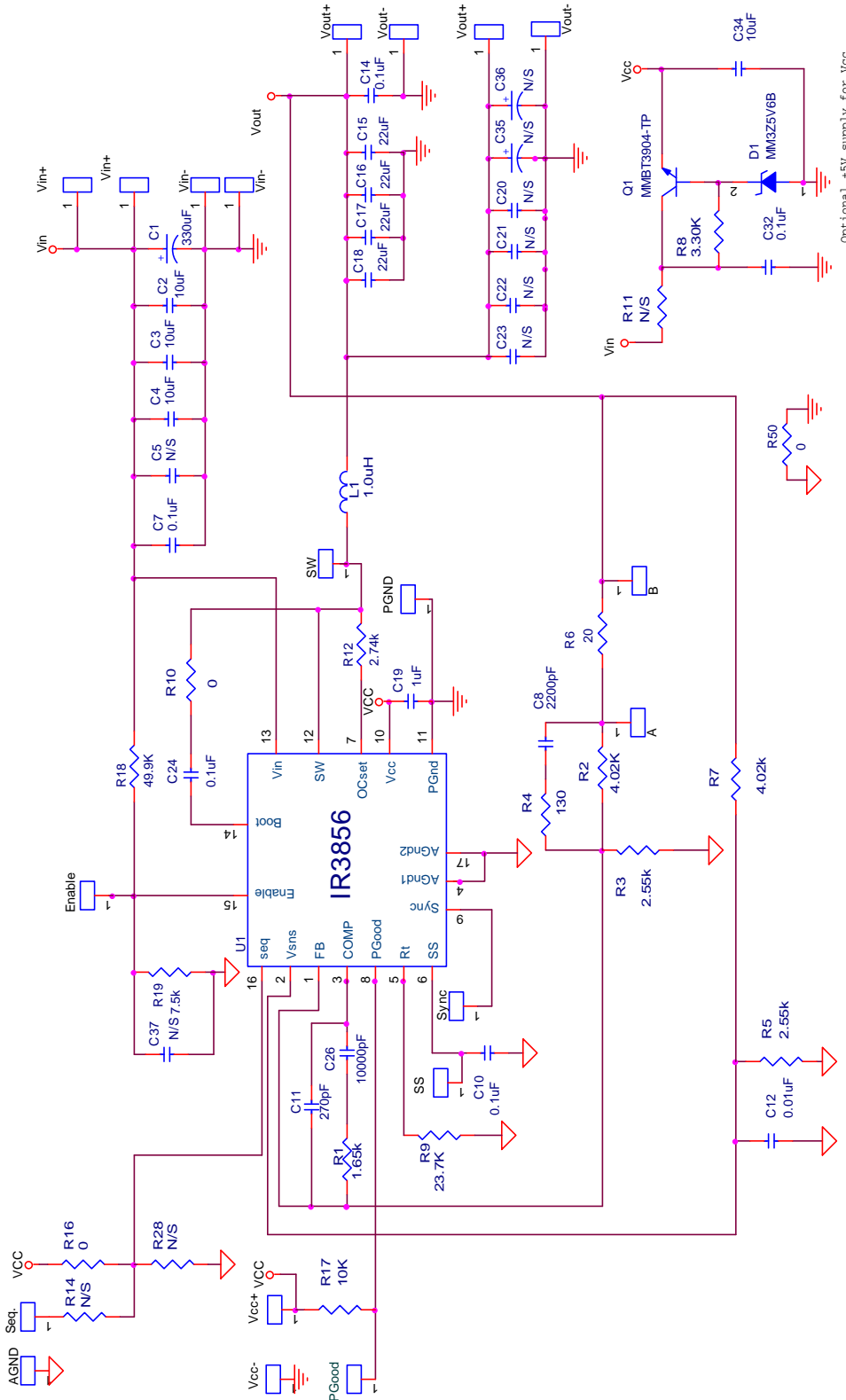


Fig. 5: Board layout, mid-layer II.



Optional +5V supply for Vcc

Single point of connection between Power
Ground and Signal ("analog") Ground

Fig. 6: Schematic of the IR3856 evaluation board

Bill of Materials

Item	Quantity	Part Reference	Value	Description	Manufacturer	Part Number
1	1	C1	330uF	SMD Electrolytic, Fsize, 25V, 20%	Panasonic	EEV-FK1E331P
2	3	C4 C3 C2	10uF	1206, 25V, X5R, 20%	Murata	GRM31CR61E106MA12L
3	1	C34	10uF	0805, 10V, X5R, 20%	TDK	C2012X5R1A106KB
4	1	C19	1uF	0603, 16V, X7R, 10%	TDK	C1608X7R1C105K
5	1	C12	0.01uF	0603, 50V, X7R, 10%	TDK	C1608X7R1H103K
6	5	C7 C10 C14 C24 C32	0.1uF	0603, 25V, X7R, 10%	TDK	C1608X7R1H104KB
7	1	C8	2200pF	0603, 50V, NP0, 5%	Murata	GRM1885C1H222JA01D
8	1	C11	270pF	0603, 50V, NP0, 5%	Murata	GRM1885C1H271JA01D
9	4	C15 C16 C17 C18	22uF	0805, 6.3V, X5R, 20%	TDK	C2012X5R0J226M
10	1	C26	10000pF	0603, 25V, X7R, 10%	TDK	C1608X7R1E103K
11	1	D1	MM3Z5V6B	MM3Z5V6B,Zener, 5.6V	Fairchild	MM3Z5V6B
12	1	L1	1.0uH	6.9x6.5x5mm, 20%, 4.7mOhm	TDK	SPM6550T-1R0M100A
13	1	Q1	MMBT3904/SOT	NPN, 40V, 200mA, SOT-23	Fairchild	MMBT3904/SOT
14	1	R8	3.3k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX3301
15	1	R18	49.9k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX4992
16	1	R4	130	Thick Film, 0603,1/10W,1%	Panasonic - ECG	ERJ-3EKF1300V
17	1	R6	20	Thick Film, 0603,1/10 W,1%	Vishey/Dale	CRCW060320R0FKEA
18	1	R9	23.7k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2372
19	3	R16 R10 R50	0	Thick Film, 0603,1/10 W,5%	Vishay/Dale	CRCW06030000Z0EA
20	1	R12	2.74k	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX2741
21	2	R3 R5	2.55k	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX2551
22	1	R17	10.0k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX1002
23	1	R19	7.50k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX7501
24	1	R1	1.65k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX1651
25	2	R2 R7	4.02k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX4021
26	1	U1	IR3856	PQFN 4mmx5mm, 6A SuplRBuck	International Rectifier	IR3856MPbF

TYPICAL OPERATING WAVEFORMS

$V_{in}=12.0V$, $V_{cc}=5V$, $V_o=1.8V$, $I_o=0-6A$, Room Temperature, No Air Flow

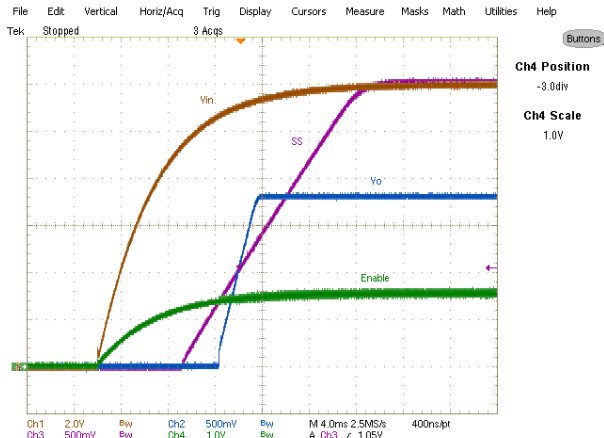


Fig. 7. Start up at 6A Load
Ch₁:V_{in}, Ch₂:V_o, Ch₃:V_{ss}, Ch₄:Enable

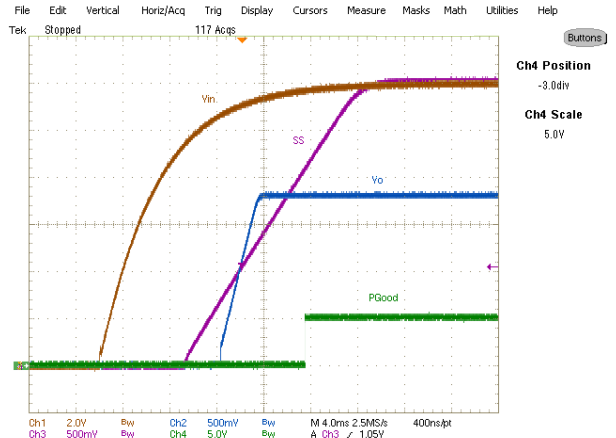


Fig. 8. Start up at 6A Load,
Ch₁:V_{in}, Ch₂:V_o, Ch₃:V_{ss}, Ch₄:V_{PGood}

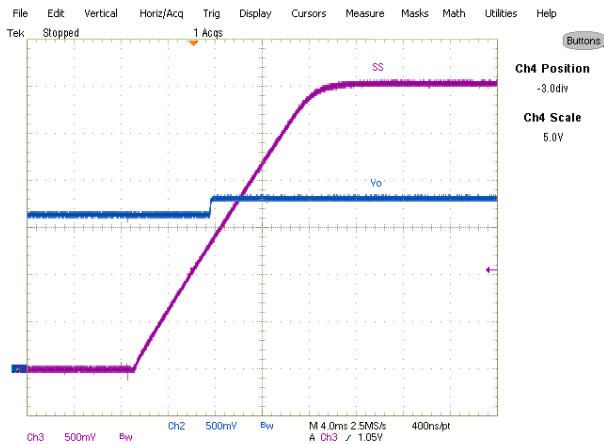


Fig. 9. Start up with 1.62V Pre Bias, 0A Load,
Ch₂:V_o, Ch₃:V_{ss}

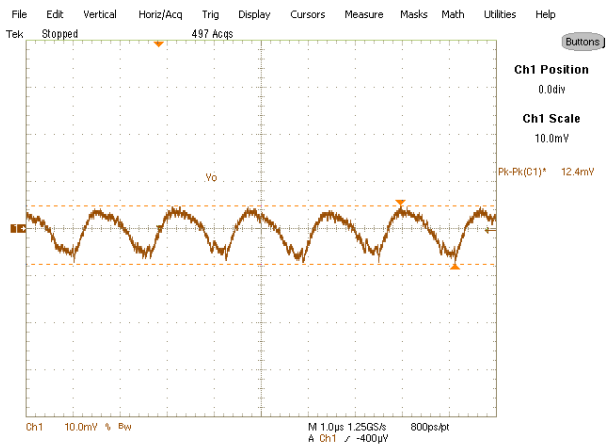


Fig. 10. Output Voltage Ripple, 6A load
Ch₁:V_o

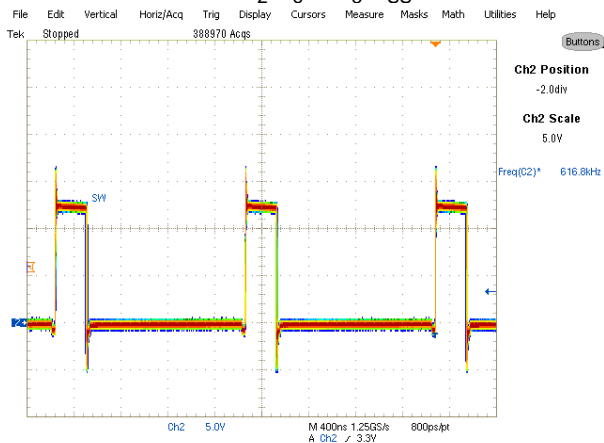


Fig. 11. Inductor node at 6A load
Ch₁:LX

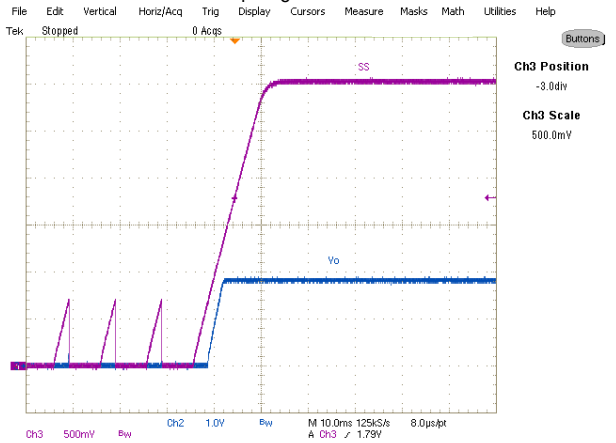


Fig. 12. Short (Hiccup) Recovery
Ch₂:V_o, Ch₃:V_{ss}

TYPICAL OPERATING WAVEFORMS

Vin=12V, Vcc=5V, Vo=1.8V, Io=0-6A, Room Temperature, No Air Flow

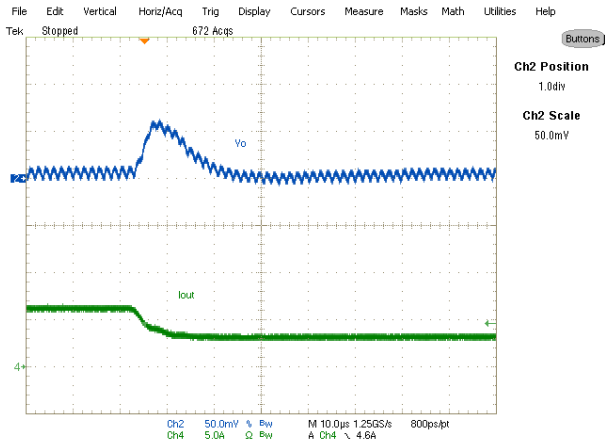
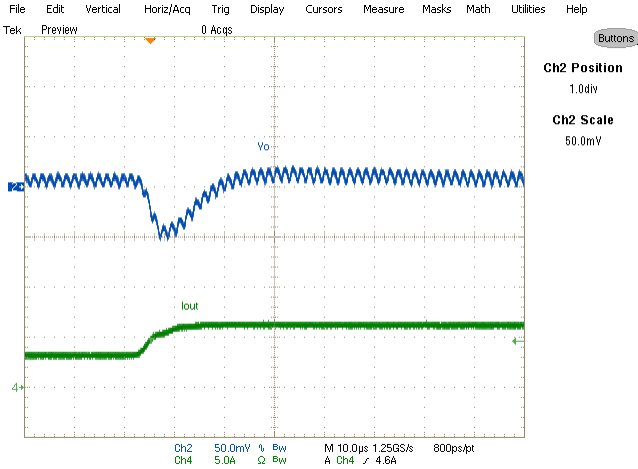
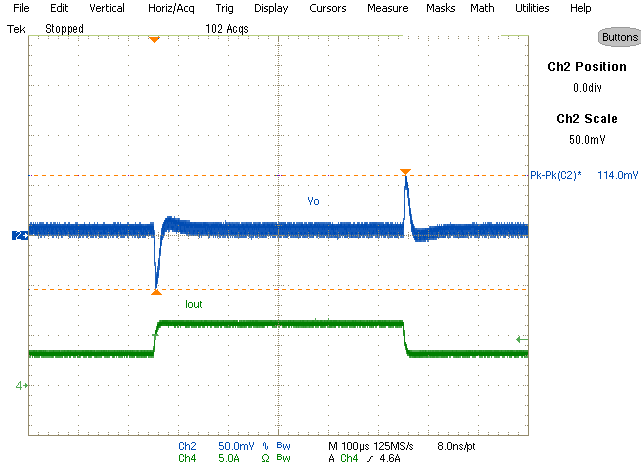


Fig. 13. Transient Response, 3A to 6A step 2.5A/µs
 Ch₂:V_o, Ch₄:I_o

TYPICAL OPERATING WAVEFORMS

Vin=12V, Vcc=5V, Vo=1.8V, Io=6A, Room Temperature, No Air Flow

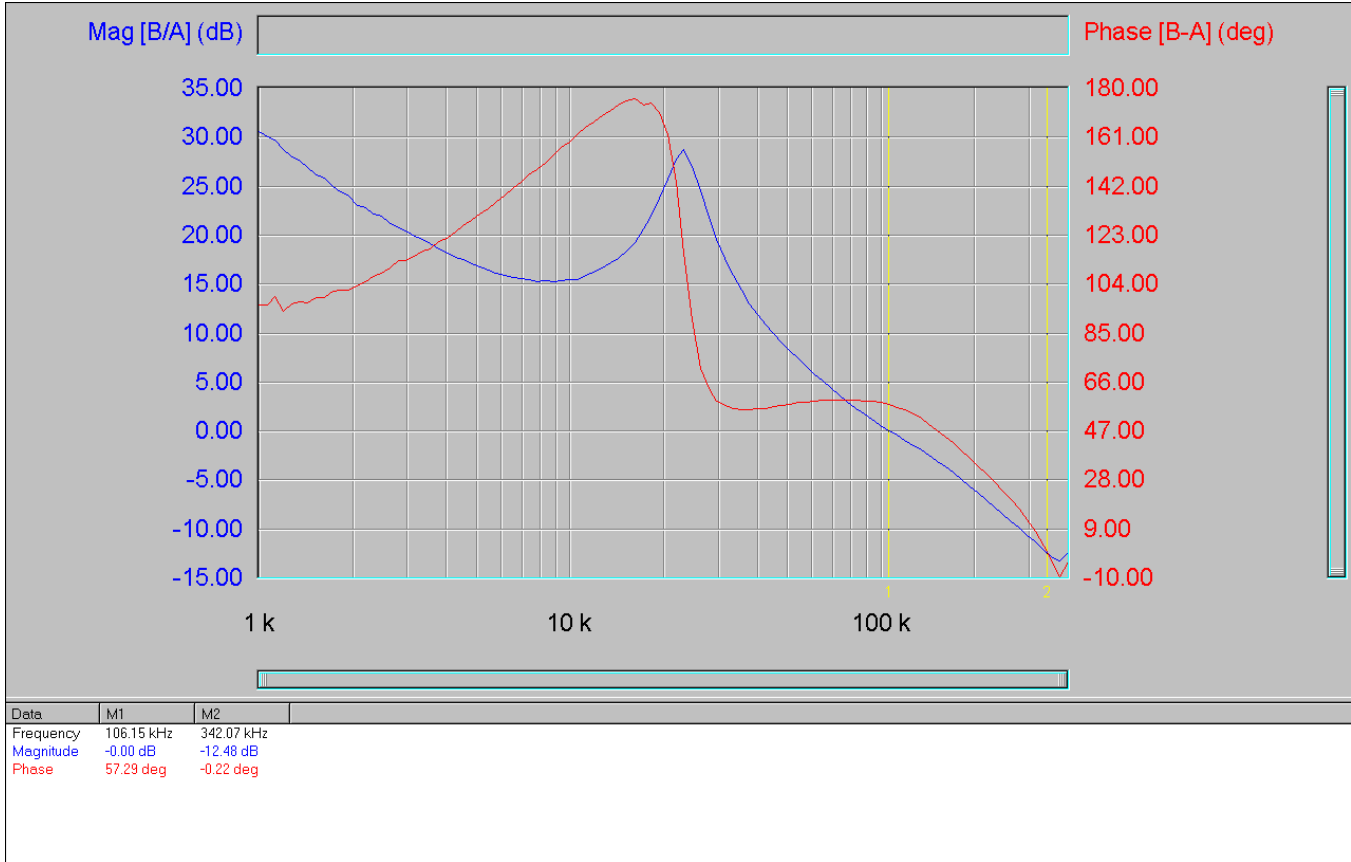


Fig. 14. Bode Plot at 6A load shows a bandwidth of 106kHz and phase margin of 57 degrees and gain margin of 12db at 342kHz

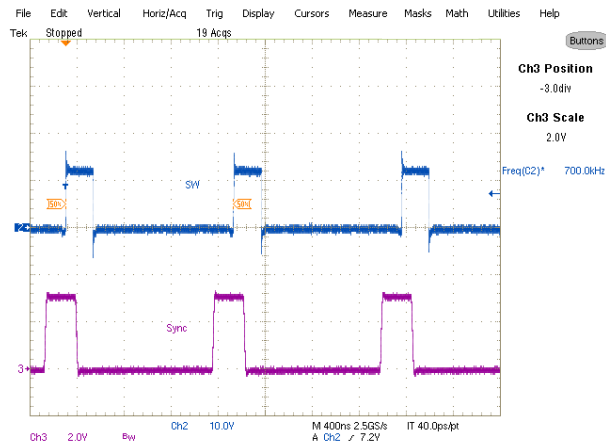


Fig. 15. Synchronization to External Clock
 Ch₂: SW node Signal, Ch₃: Sync. Pin

TYPICAL OPERATING WAVEFORMS

$V_{in}=12V$, $V_o=1.8V$, $I_o=0-6A$, Room Temperature, No Air Flow

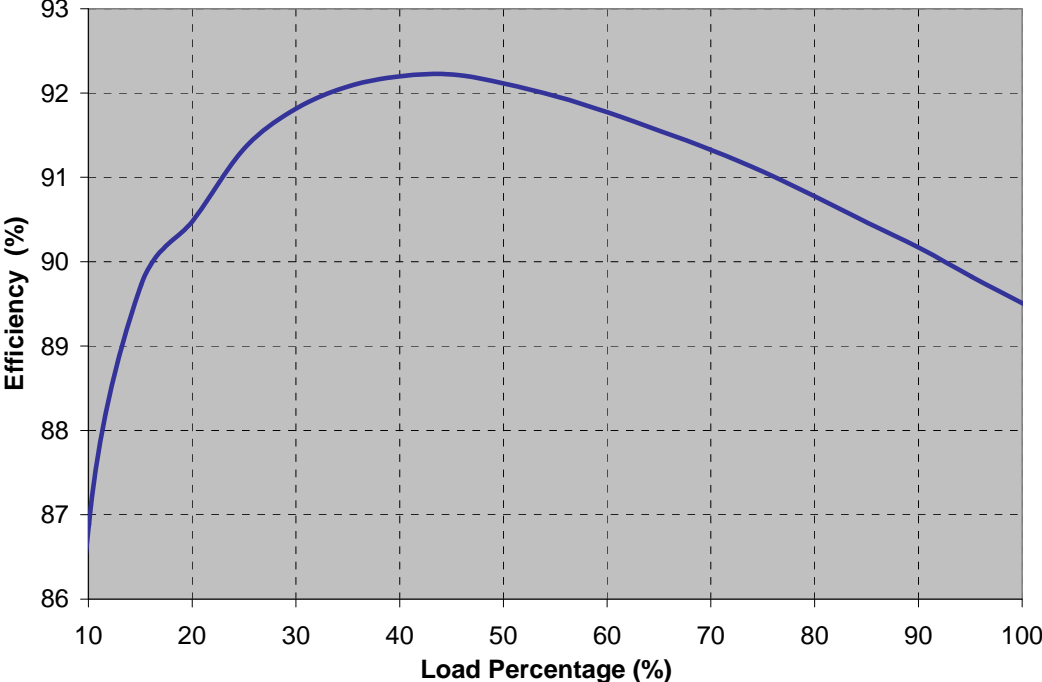


Fig.16: Efficiency versus load current

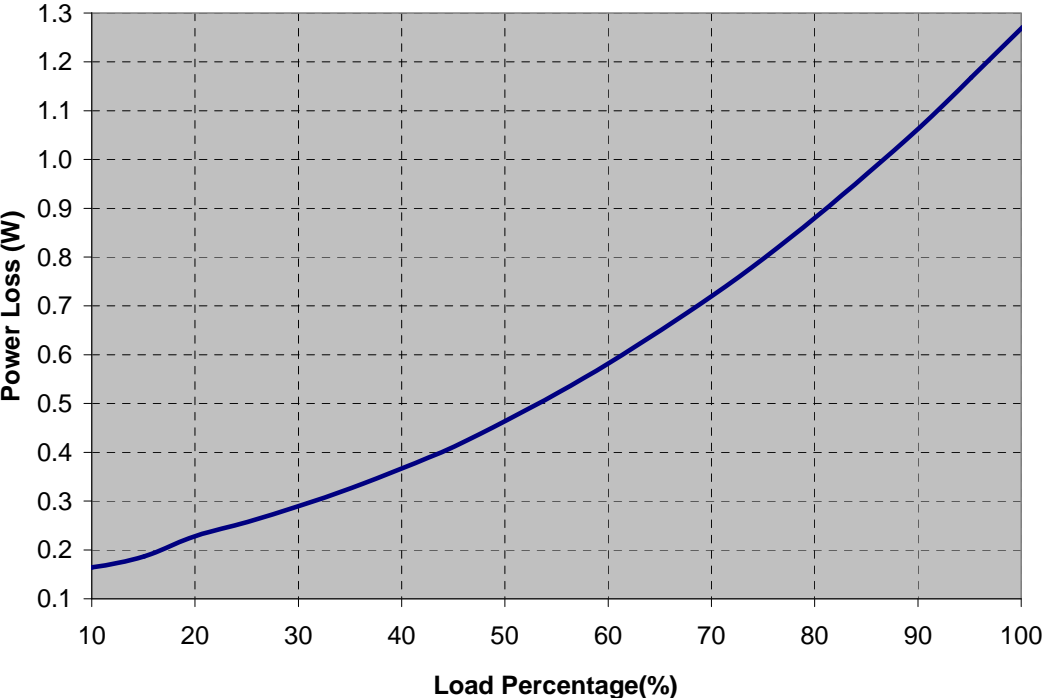


Fig.17: Power loss versus load current

THERMAL IMAGES

Vin=12V, Vo=1.8V, Io=6A, Room Temperature, No Air Flow



Fig. 18: Thermal Image at 6A load
Test points 1 and 2 are IR3856 and inductor, respectively.

Simultaneous Tracking at Power Up and Power Down
Vin=12V, Vo=1.8V, Io=6A, Room Temperature, No Air Flow

In order to run the IR3856 in the simultaneous tracking mode, the following steps should be taken:

- Remove R16 from the board.
- Set the value of R14 and R28 as R2 (4.02K) and R3 (2.55K), respectively.
- Connect the controlling input across SEQ and AGND test points on the board. This voltage should be at least 1.15 time greater than Vo. For the following test results a 0-3.3V source is applied to SEQ input.
- The controlling input should be applied after the SS pin is clamped to 3.0V.

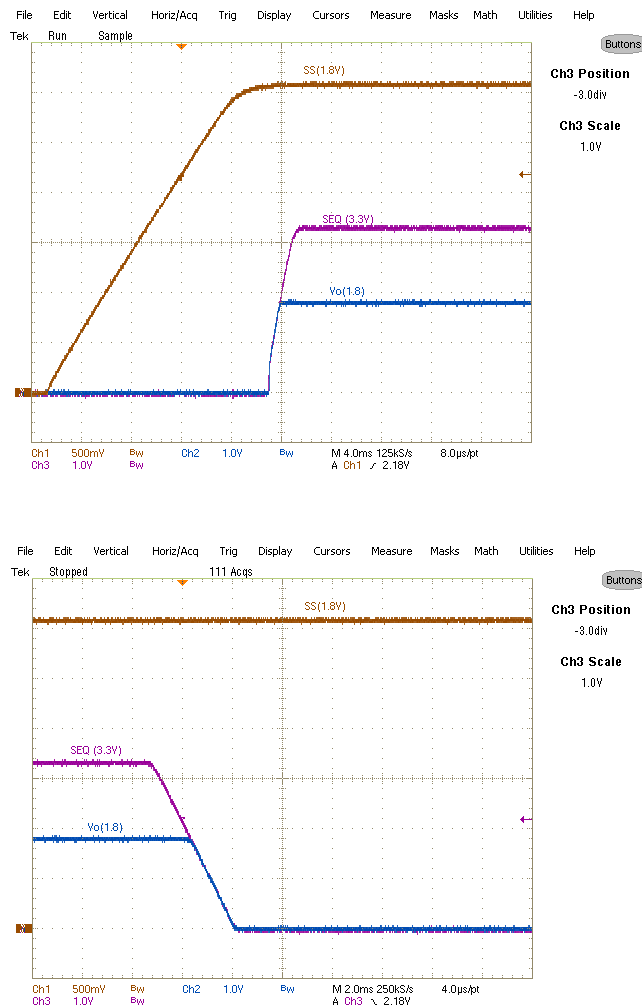
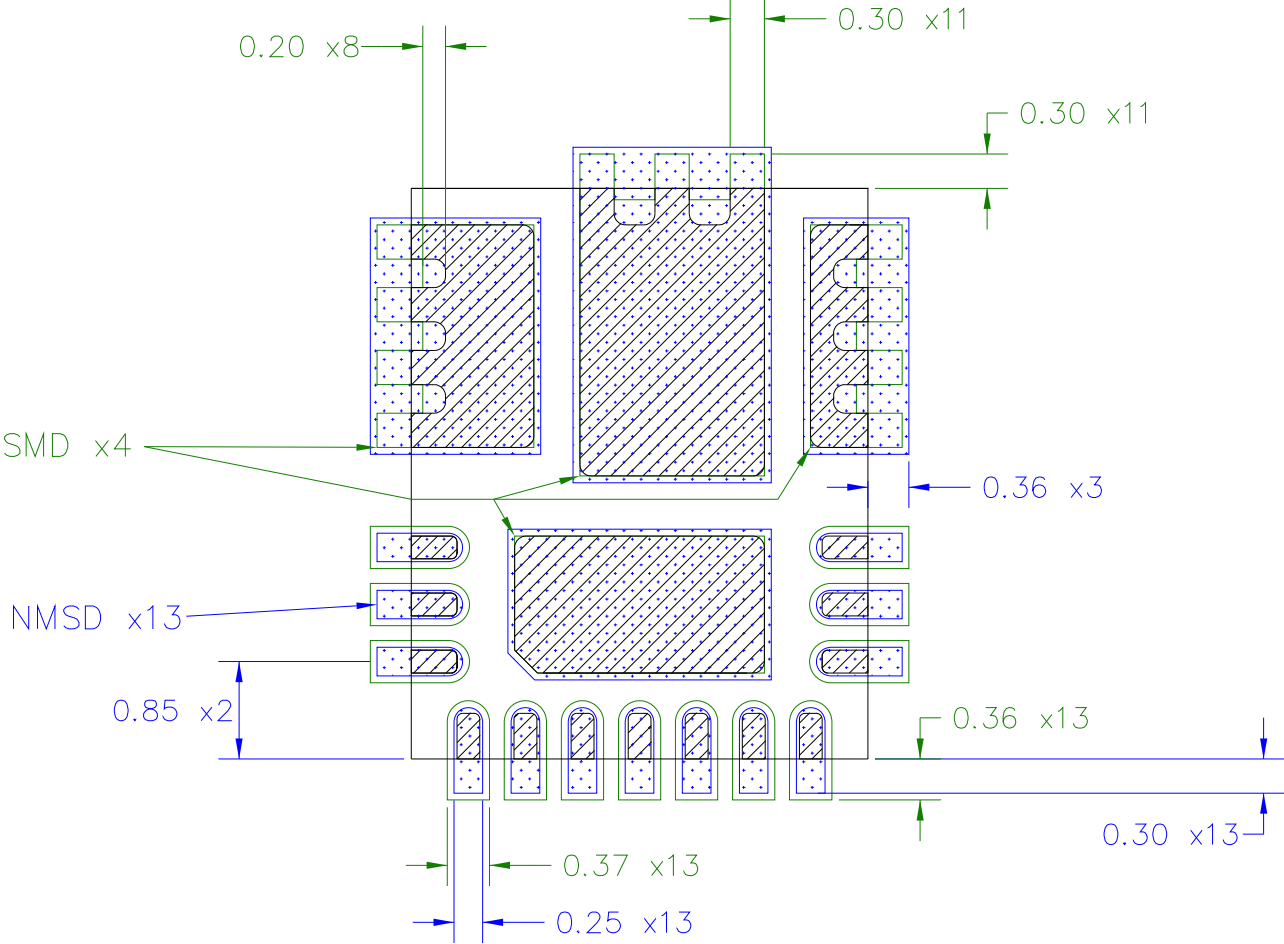





Fig. 19: Simultaneous Tracking a 3.3V input at power-up and shut-down
 Ch1: SS (1.8V) Ch2:Vout (1.8V) Ch3: SEQ (3.3V)

PCB Metal and Components Placement

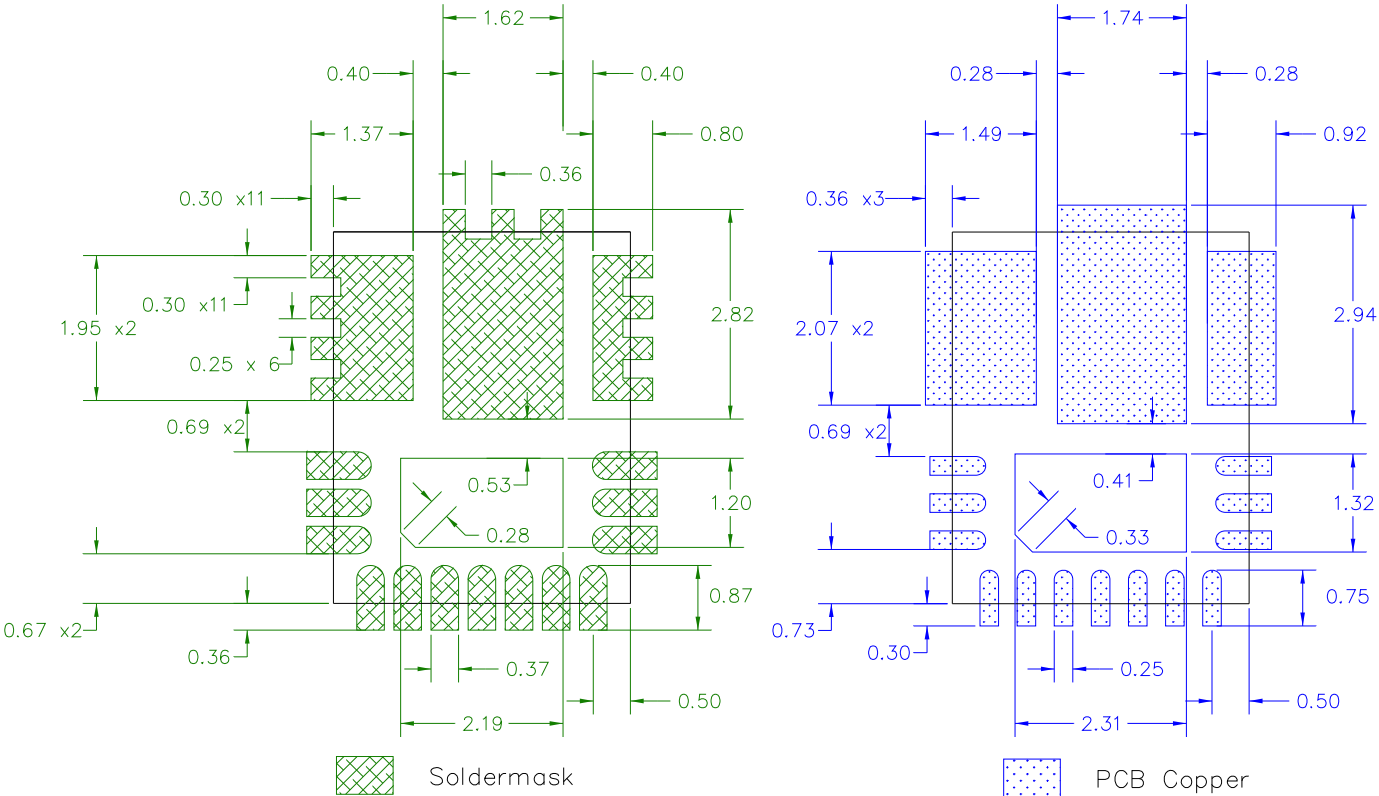


All Dimensions in mm

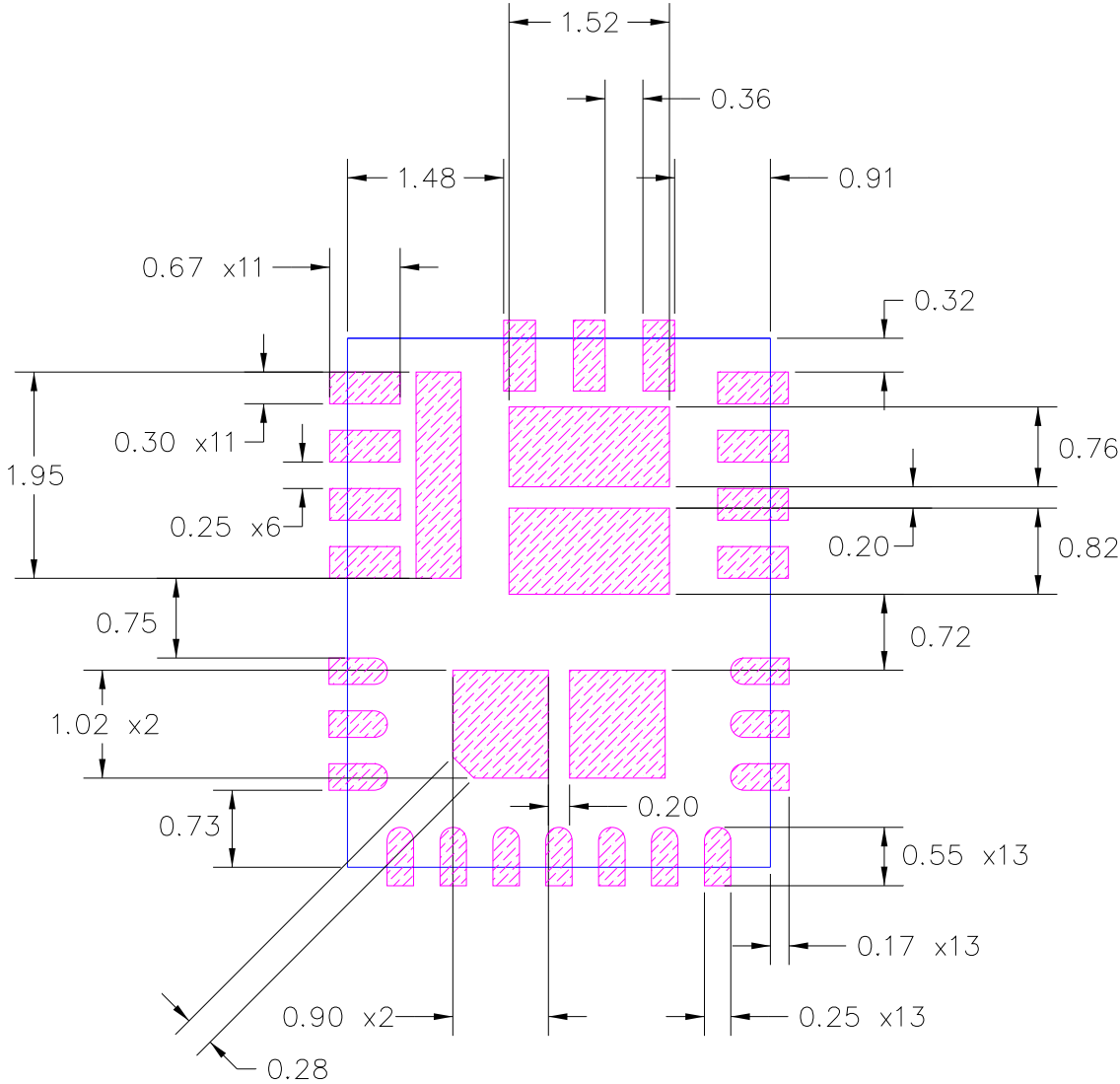
-  PCB Copper
-  Component
-  Soldermask

Solder Resist

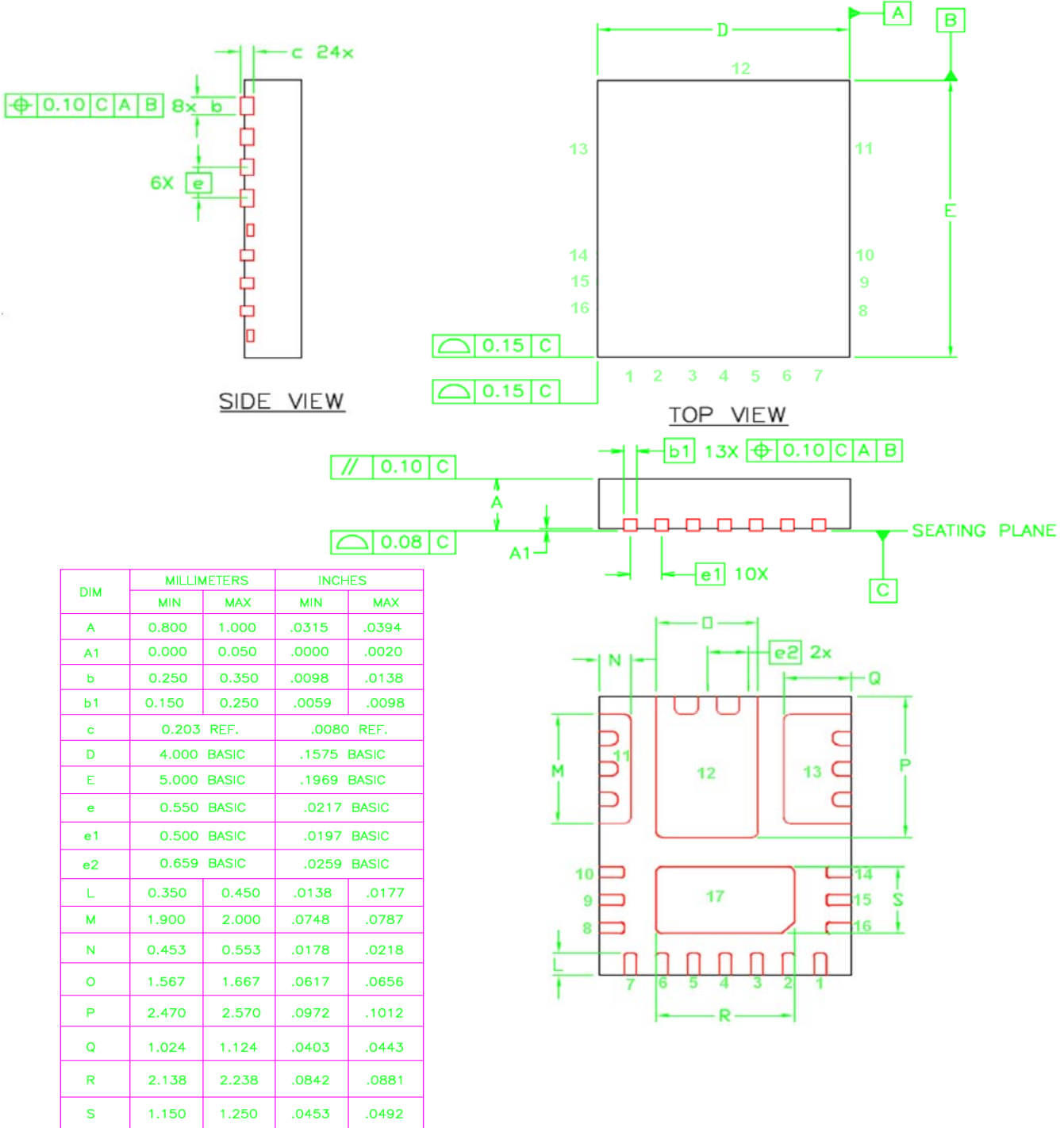
All Dimensions in mm



Stencil Design



Stencil Aperture
All Dimensions in mm



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

This product has been designed and qualified for the Consumer market

Visit us at www.irf.com for sales contact information

Data and specifications subject to change without notice. 06/10