PIC16(L)F1615/1619 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1615/1619 family devices that you have received conform functionally to the current Device Data Sheet (DS40001770**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1615/1619 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 3, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1615/1619 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1,2)	
	DEV<8:0>	Revision ID for Silicon Revision
		A4
PIC16F1615	307Ch	4h
PIC16LF1615	307Eh	4h
PIC16F1619	307Dh	4h
PIC16LF1619	307Fh	4h

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC12(L)F1612/16(L)F161X Memory Programming Specification"* (DS40001720) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A4
None	N/A	N/A	No known issues	N/A

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

None.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001770**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: eXtreme Low-Power (XLP) Features

The line stating:

- Secondary Oscillator: 500 nA @ 32 kHz

should be removed. This device does not have a secondary oscillator feature.

2. Module: Electrical Characteristics

Parameters D080A and D090A should be as follows:

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
	VOL	**Output Low Voltage(3)**					
D080A		High Drive I/O(1)	—	2.5V	—	V	IOL = 100 mA, VDD = 5.0V
	VOH	**Output High Voltage(3)**					
D090A		High Drive I/O(1)	—	2.5V	—	V	IOL = 100 mA, VDD = 5.0V

3. Module: Electrical Characteristics

Parameter OS08 should be as follows:

Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Sym.**	**Characteristic**	**Freq. Tolerance**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(1)	—	—	16.0	—	MHz	**(Note 2)**

4. Module: Electrical Characteristics

For Table 35-8, Note 2 should read as follows:

2: See Figure 35-6: "HFINTOSC Frequency Accuracy over Device VDD and Temperature".

5. Module: Electrical Characteristics

Table 35-17 Parameters ZC02 and ZC03 should be as follows:

Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
ZC02	ZCSRC	Source current	—	-300	-600	μA	
ZC03	ZCSNK	Sink current	—	300	600	μA	

6. Module: DC and AC Characteristics Graphs and Charts

The following two graphs should be added to the graphs:

FIGURE 36-7: VOH vs. IOH OVER TEMPERATURE FOR HIGH DRIVE PINS, VDD = 5.0V

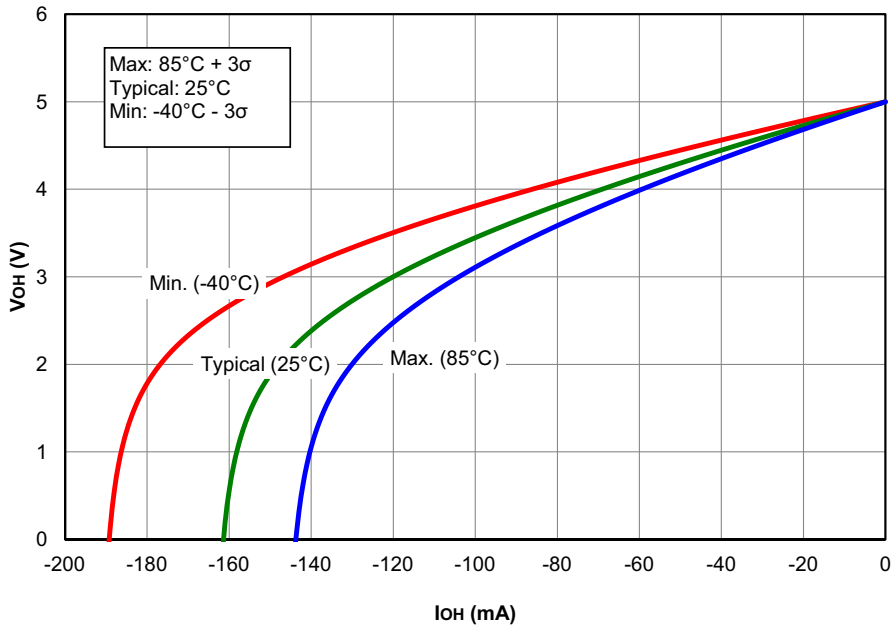
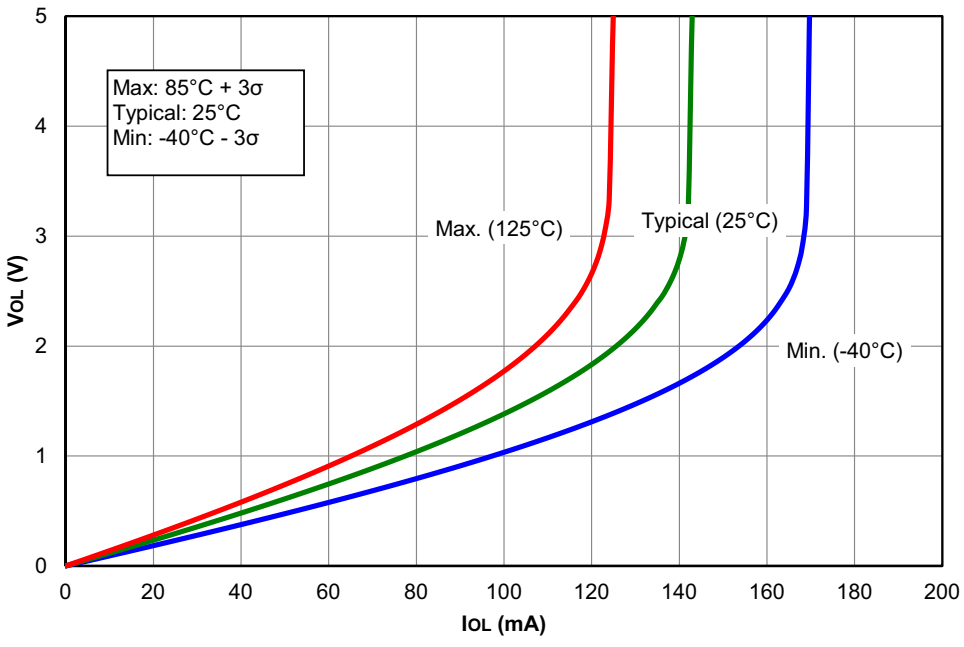


FIGURE 36-8: VOL vs. IOL OVER TEMPERATURE FOR HIGH DRIVE PINS, VDD = 5.0V



7. Module: DC and AC Characteristics Graphs and Charts

Figures 36-29 and 36-30 graphs should be removed from the document

8. Module: PPS

Table 13-2 should be as follows:

TABLE 13-2: AVAILABLE PORTS FOR OUTPUT BY PERIPHERAL(2)

RxyPPS<4:0>	Output Signal	PIC16(L)F1618			PIC16(L)F1614	
		PORTA	PORTB	PORTC	PORTA	PORTC
11xxx	Reserved	●	●	●	●	●
10111	Reserved	●	●	●	●	●
10110	Reserved	●	●	●	●	●
10101	Reserved	●	●	●	●	●
10100	Reserved	●	●	●	●	●
10011	**DT**	●	●	●	●	●
10010	**TX/CK**	●	●	●	●	●
10001	SDO/SDA(1)	●	●	●	●	●
10000	SCK/SCL(1)	●	●	●	●	●
01111	PWM4_out	●	●	●	●	●
01110	PWM3_out	●	●	●	●	●
01101	CCP2_out	●	●	●	●	●
01100	CCP1_out	●	●	●	●	●
01011	CWG1OUTD(1)	●	●	●	●	●
01010	CWG1OUTC(1)	●	●	●	●	●
01001	CWG1OUTB(1)	●	●	●	●	●
01000	CWG1OUTA(1)	●	●	●	●	●
00111	**LC4**	●	●	●	●	●
00110	**LC3**	●	●	●	●	●
00101	LC2_out	●	●	●	●	●
00100	LC1_out	●	●	●	●	●
00011	ZCD1_out	●	●	●	●	●
00010	sync_C2OUT	●	●	●	●	●
00001	sync_C1OUT	●	●	●	●	●
00000	LATxy	●	●	●	●	●

Note 1: TRIS control is overridden by the peripheral as required.

2: Unsupported peripherals will output a '0'.

9. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):

Section 25.4.2 should read as follows:

During the course of automatic baud detection, the ABDOVF bit of the BAUDxCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPxBRGH:SPxBRGL register pair. The overflow condition will set the RCIF flag. The counter continues to count until the fifth rising edge is detected on the RX pin. **The RCIDL bit will remain false ('0') until the fifth rising edge at which time the RCIDL bit will be set. If the RCREG is read after the overflow occurs but before the fifth rising edge then the fifth rising edge will set the RCIF again. Terminating the auto-baud process early to clear an overflow condition will prevent proper detection of the sync character fifth rising edge. If any falling edges of the sync character have not yet occurred when the ABDEN bit is cleared then those will be falsely detected as Start bits. The following steps are recommended to clear the overflow condition:**

1. **Read RCREG to clear RCIF.**
2. **If RCIDL is zero then wait for RCIF and repeat step 1.**
3. **Clear the ABDOVF bit**

10. Module: Comparator

Register 19-1 should be as follows:

REGISTER 19-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R-0/0	U/U-0/0	R/W-0/0	U-0	R/W-1/1	R/W-0/0	R/W-0/0
CxON	CxOUT	—	CxPOL	—	CxSP	CxHYS	CxSYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **CxON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled and consumes no active power

bit 6 **CxOUT:** Comparator Output bit
If CxPOL = 1 (inverted polarity):
1 = CxVP < CxVN
0 = CxVP > CxVN
If CxPOL = 0 (non-inverted polarity):
1 = CxVP > CxVN
0 = CxVP < CxVN

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **CxPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **CxSP:** Comparator Speed/Power Select bit
1 = Comparator operates in normal power, higher speed mode
0 = Comparator operates in Low-power, Low-speed mode

bit 1 **CxHYS:** Comparator Hysteresis Enable bit
1 = Comparator hysteresis enabled
0 = Comparator hysteresis disabled

bit 0 **CxSYNC:** Comparator Output Synchronous Mode bit
1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source.
0 = Comparator output to Timer1 and I/O pin is asynchronous

11. Module: Capture/Compare/PWM Modules

Section 26.1.6 Capture Output should read as follows:

26.1.6 CAPTURE OUTPUT

Whenever a capture occurs, the output of the CCP will go high for a period equal to one system clock period (1/FOSC). This output is available as an input signal to the CWG, as an auto-conversion trigger for the ADC, as an External Reset Signal for the TMR2 modules, as a window input to the SMT, and as an input to the CLC module. In addition, **the CCPx pin output can be mapped to output pins through the use of PPS (see 13.2 "PPS Outputs").**

12. Module: Capture/Compare/PWM Modules

Section 26.2.5 Capture Output should read as follows:

26.2.5 CAPTURE OUTPUT

When in Compare mode, the CCP will provide an output upon the 16-bit value of the CCPRxH:CCPRxL register pair matching the TMR1H:TMR1L register pair. The compare output depends on which Compare mode the CCP is configured as. If the MODE bits of CCPxCON register are equal to '1011' or '1010', the CCP module will output high, while TMR1 is equal to CCPRxH:CCPRxL register pair. This means that the pulse width is determined by the TMR1 prescaler. If the MODE bits of CCPxCON are equal to '0001' or '0010', the output will toggle upon a match, going from '0' to '1' or vice-versa. If the MODE bits of CCPxCON are equal to '1001', the output is cleared on a match, and if the MODE bits are equal to '1000', the output is set on a match. This output is available as an input signal to the CWG, as an auto-conversion trigger for the ADC, as an external Reset signal for the TMR2 modules, as a window input to the SMT, and as an input to the CLC module. In addition, **the CCPx pin output can be mapped to output pins through the use of PPS (see 13.2 "PPS Outputs").**

13. Module: Capture/Compare/PWM Modules

Section 26.4.7 PWM Output should read as follows:

26.4.7 PWM OUTPUT

The output of the CCP in PWM mode is the PWM signal generated by the module and described above. This output is available as an input signal to the CWG, as an auto-conversion trigger for the ADC, as an external Reset signal for the TMR2 modules, as a window input to the SMT, and as an input to the CLC module. In addition, **the CCPx pin output can be mapped to output pins through the use of PPS (see 13.2 "PPS Outputs").**

14. Module: Capture/Compare/PWM Modules

Register 26-1 should be as follows:

REGISTER 26-1: CCPxCON: CCPx CONTROL REGISTER

R/W-0/0	U/U-0/0	R-x	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	OUT	FMT	MODE<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **EN:** CCPx Module Enable bit
1 = CCPx is enabled
0 = CCPx is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **OUT:** CCPx Output Data bit (read-only)

bit 4 **FMT:** CCPW (Pulse-Width) Alignment bit
If MODE = PWM Mode
1 = Left-aligned format, CCPRxH <7> is the MSB of the PWM duty cycle
0 = Right-aligned format, CCPRxL<0> is the LSB of the PWM duty cycle

bit 3-0 **MODE<3:0>:** CCPx Mode Selection bit
11xx = PWM mode

1011 = Compare mode: Pulse output, clear TMR1
1010 = Compare mode: Pulse output (0 - 1 - 0)
1001 = Compare mode: clear output on compare match
1000 = Compare mode: set output on compare match

0111 = Capture mode: every 16th rising edge
0110 = Capture mode: every 4th rising edge
0101 = Capture mode: every rising edge
0100 = Capture mode: every falling edge

0011 = Capture mode: every rising or falling edge
0010 = Compare mode: toggle output on match
0001 = Compare mode: Toggle output and clear TMR1 on match
0000 = Capture/Compare/PWM off (resets CCPx module) (reserved for backwards compatibility)

15. Module: Complimentary Waveform Generator (CWG) Module

Register 28-8 should be removed.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2014)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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