i.MX31-10 SOM-LV Hardware Specification

Hardware Documentation

Logic // Embedded Product Solutions
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Revision History

REV	EDITOR	REVISION DESCRIPTION	Schematic PN & REV	APPROVAL	DATE
1	KTL	Internal Release	1004734 Rev 4	JCA	08/16/06
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B	KTL, JCA	General grammatical and formatting changes; Added PRELIMINARY watermark; Updated Figure 1.2, SOM-LV block diagram; Updated SOM-LV Mechanical Drawings and added recommend PCB layout drawing; Added SD memory to 2.3.3 NOR Flash; Section 3.1 Configuration: added 0 to NOR flash options; The following schematic updates from beta debug: - J1 Pin# 23, 37 changed to 3.3V; - J1 Pin# 114 changed to memory mode only; J1 table added note 2; - Updated netname in parenthses for J1 Pin# 185, 187, 191, 193, 195, 211, 213, 215, 217, 219, and J2 Pin# 182, 188; - Updated J2 Pin# 13, 15 from No connect to current signal name; - Updated J2 Pin# 14 Description	1004734 Rev 6	KTL	02/20/07
C	JCA	- Removed PRELIMINARY watermark; - Removed “SOM Advantages” Section; - Section 4: Changed “CDS0” and “CDS1” to “CSD0” and “CSD1”; - Section 5.2: Change pin# 152 from “LCD_LCS1” to “PCC_POWER_nEN”; - Throughout: Updated “SOM” references to the form factor-specific “SOM-LV”; General grammatical and formatting changes	1004734 Rev 6	KTL	04/25/07
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F	JCA	- Added standard document cover page; updated header and footer layout; - Section 1.6.1.1: Values for typical currents were given in Amps when they should be in mA, this has been corrected for all of the current values in the table; Corrected extended temperature lower limit, was -20, should be -30; - Section 2.11: Corrected bits in offset column for FAST_nCS, was 0x01000000, should be 0x00800000; - Section 3.6.1.1: Removed reference to MC13783 Users Guide; - Section 3.6.1.2: Updated all text in the section; - Sections 5.1 & 5.2: Updated all signals listed as “NC – no connect” to “RFU – reserve for future use; - Section 5.1: Corrected voltages for J1 Pin# 25 (USB1_PWR_nEN) and J1 Pin# 39 (USB2_PWR_nEN), were 5.0V, should be 3.3V; J1 Pin# 53 corrected voltage, was 1.8V, should be GND; - Section 5.2: Updated J2 Pin# 93 from “KEY_COL7” to	1004734 Rev 11	BB, TED, & JCA	08/29/08

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REV	EDITOR	REVISION DESCRIPTION	Schematic PN & REV	APPROVAL	DATE
		"PCC_PCMCIA_nEN"; - Section 6: Replaced the in-text mechanical drawings with two pages of mechanical drawings; Corrected hole dimension tolerance, was ±0.01 mm, should be ±0.08 mm			
G	JCA	- Section 1.1: Replaced Product Brief with Product Overview text; - Section 5.1: Corrected voltage references for UARTC signals J1.122, J1.124, J1.126, & J1.128; - Added Section 6.2 "Mounting Specifications" - Section 6.3: Updated footprint dimensioning scheme in drawing	1004734 Rev 11	JCA	03/20/09

Please check www.logicpd.com/auth/downloads/i.MX31/ for the latest revision of this specification, product change notifications, and additional documentation for the i.MX31 SOM-LV.

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1 Introduction

1.1 Product Overview

The i.MX31 System on Module (SOM) is a compact, productready hardware and software solution that fast forwards your embedded product design.

Designed in the SOM-LV form factor, the i.MX31 module offers essential features for handheld and embedded networking applications. Use of custom baseboards makes the SOM-LV the ideal foundation for OEMs developing handheld and compact products. The SOM-LV provides a common reference pin-out on its expansion connectors, which enables easy scalability when new functionality or performance is required.

Application development is performed right on the product-ready i.MX31 SOM-LV and software Board Support Packages (BSPs), which enables you to seamlessly transfer your application code and hardware into production.

The i.MX31 SOM-LV is ideal for applications in the medical, point-of-sale, industrial, and security markets. From patient monitoring and medical imaging, to card payment terminals and bar code readers, to CCTV cameras and intruder alarms, the i.MX31 SOM-LV allows for powerful versatility and long-life products.

1.2 Acronyms

ADC	Analog to Digital Converter
BSP	Board Support Package
BTB	Board-to-Board
CCM	Clock Controller Module
CSPI	Configurable Serial Peripheral Interface
DDR	Double Data Rate (RAM)
DMA	Direct Memory Access
ECB	Event Control Block
ESD	Electrostatic Discharge
FIFO	First In First Out
GPIO	General Purpose Input Output
GPO	General Purpose Output
HR-TFT	High Reflective-Thin Film Transistor (LCD)
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Circuit Sound
IC	Integrated Circuit
IDC	Insulation Displacement Connector
I/O	Input/Output
IRQ	Interrupt Request
ISA	Industry Standard Architecture
LCD	Liquid Crystal Display
LDO	Low Dropout (Regulator)
LoLo	LogicLoader™
OTG	On-the-Go (USB)
PCB	Printed Circuit Board
PCMCIA	Personal Computer Memory Card Internation Association (PC Cards)
PHY	Physical Layer
PLL	Phase Lock Loop
PWM	Pulse Width Modulation
RTC	Real Time Clock
SDIO	Secure Digitial Input Output

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SDRAM	Synchronous Dynamic Random Access Memory
SOM	System on Module
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
STN	Super-Twisted Nematic (LCD)
TFT	Thin Film Transistor (LCD)
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
WEIM	Wireless External Interface Module

1.3 Scope of Document

This Hardware Specification is unique to the design and use of the i.MX31-10 SOM-LV as designed by Logic and does not intend to include information outside of that scope. Detailed information about the Freescale i.MX31 processor or any other device component on the SOM can be found in their respective manuals and specification documents. Specific documents mentioned within this Hardware Specification include:

- LogicLoader User's Manual (available from Logic at www.logicpd.com/auth/)
- i.MX31-10 SOM-LV Schematics (available from Logic at www.logicpd.com/auth/)
- i.MX31 Reference Manual (available from Freescale® at www.freescale.com/iMX)
- i.MX31 Data Sheet (available from Freescale at www.freescale.com/iMX)
- MC13783 Data Sheet (available from Freescale's website)
- USB 2.0 Specification (available from USB.org at www.usb.org/developers/docs/)

1.4 SOM-LV Interface

Logic's common SOM-LV interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common SOM-LV footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information.

In fact, encapsulating a significant amount of your design onto the SOM-LV reduces any long-term risk of obsolescence. If a component on the SOM-LV design becomes obsolete, Logic will simply design for an alternative part that is transparent to your product. Furthermore, Logic tests all SOMs prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.

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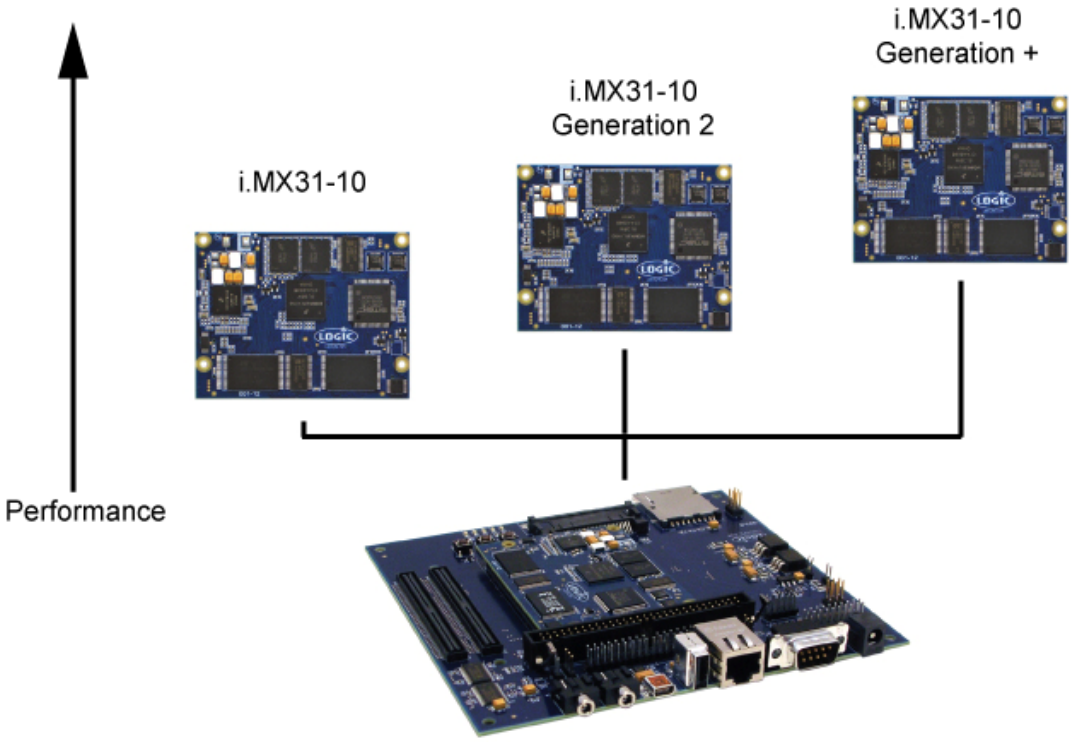

Figure 1.1: SOM-LV Advantages

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1.5 i.MX31-10 SOM-LV Block Diagram

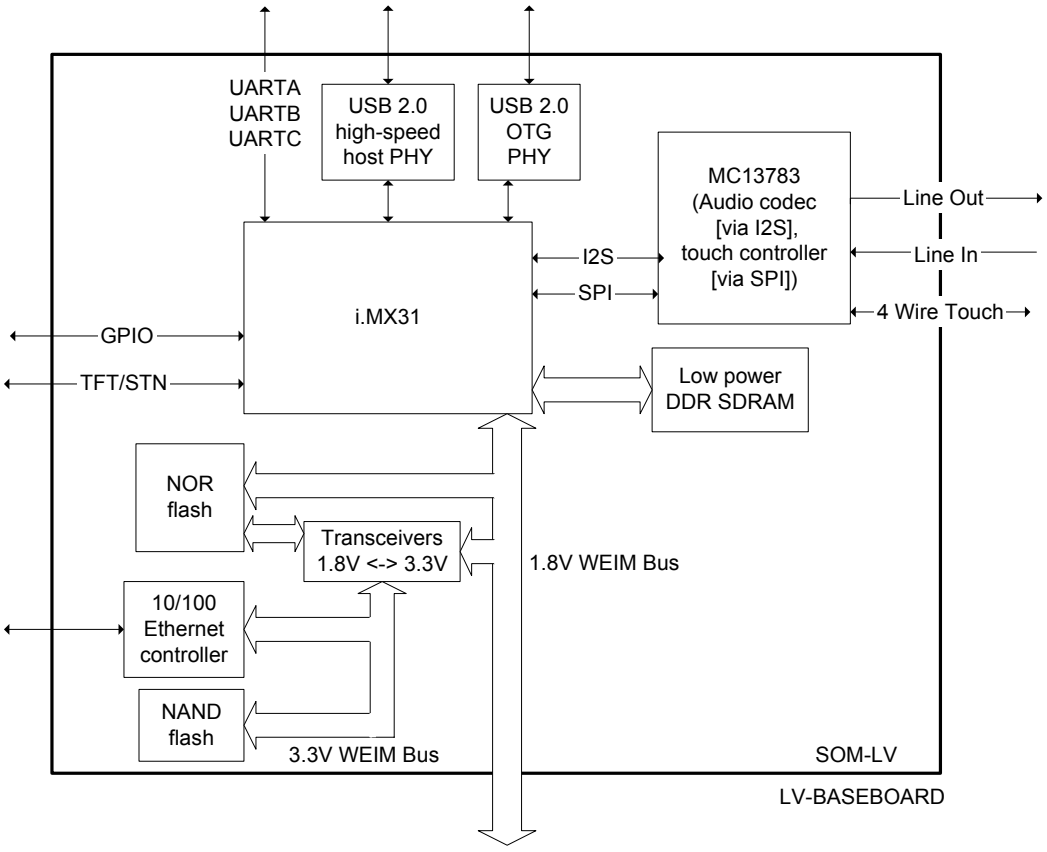

Figure 1.2: i.MX31-10 SOM-LV Block Diagram

1.6 Electrical, Mechanical, and Environmental Specifications

1.6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC 3.3 V Supply Voltage	3.3V_IN	VSS-0.3 to 3.6	V
DC Main Battery Input Voltage	MAIN_BATTERY	VSS-0.3 to 4.65	V
RTC Backup Battery Voltage	3.3V_uP_BATT	VSS-0.3 to 4.65	V

NOTE: These stress ratings are only for transient conditions. Operation at, or beyond, absolute maximum rating conditions may affect reliability and cause permanent damage to the SOM-LV and its components.

1.6.1.1 Recommended Operating Conditions

CPU power rails are sequenced on the module. The following numbers are based on tests conducted with a standard i.MX31 SOM-LV (MIMX31CSOM) and standard LV-Baseboard included with the i.MX LITEKIT. These tests try to exclude peripheral current consumption as much as possible; therefore, no peripherals (e.g., cables, devices, LCD) are connected to the board during the test.

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Parameter	Min	Typical	Max	Unit	Notes
DC Main Battery Input Voltage	2.7	3.3	4.2	V	
DC Main Battery Active Current (2)	—	310	—	mA	1, 2
DC Main Battery Active Current (3)	—	310	—	mA	1, 3
DC Main Battery Active Current (4)	—	288	—	mA	1, 4
DC Main Battery Idle Current	—	112	—	mA	1, 5
DC Main Battery Suspend Current	—	18	—	mA	1, 6
DC 3.3 V Voltage	3.0	3.3	3.6	V	
DC 3.3 V Active Current (2)	—	136	—	mA	1, 2
DC 3.3 V Active Current (3)	—	206	—	mA	1, 3
DC 3.3 V Active Current (4)	—	122	—	mA	1, 4
DC 3.3 V Idle Current	—	118	—	mA	1, 5
DC 3.3 V Suspend Current	—	124	—	mA	1, 6
Commercial Operating Temperature	0	25	70	°C	
Extended Operating Temperature	-30	—	85	°C	
Storage Temperature	-40	25	85	°C	
Dimensions	—	59.1 x 76.2 x 7.9	—	mm	
Weight	—	25.5	—	Grams	7
Connector Insertion/Removal	—	50	—	Cycles	8
Input Signal High Voltage	0.7 x VREF	—	VREF	V	9
Input Signal Low Voltage	GND	—	0.3 x VREF	V	9
Output Signal High Voltage	0.8 x VREF	—	VREF	V	9
Output Signal Low Voltage	GND	—	0.2 x VREF	V	9

Notes:

1. Processor running at 400 MHz.
2. Full Run [Active], while(1) loop in LogicLoader. No peripherals attached.
3. Full Run [Active], while(1) loop in LogicLoader with Ethernet enabled and cable attached. No peripherals attached except Ethernet cable.
4. WinCE Running FloatingPoint application. No peripherals attached.
5. WinCE Idle. No peripherals attached.
6. WinCE Suspend. No peripherals attached.
7. May vary depending on SOM-LV configuration.
8. Based on connector manufacturer’s specification.
9. VREF represents the peripheral IO supply reference for the specific CPU voltage rail.

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2 Electrical Specification

2.1 Microcontroller

2.1.1 i.MX31 Microcontroller

The i.MX31-10 SOM-LV uses Freescale's highly integrated i.MX31 processor. This device features the ARM1136JF-S core and provides many integrated on-chip peripherals, including:

- Integrated ARM1136JF-S Core
  - 32-bit ARM 11 core
  - Vectored floating point unit
  - 32x16 MAC
  - 16 Kbytes instruction cache
  - 16 Kbytes data L1 cache
  - 128 Kbyte L2 cache
  - 16 Kbyte SRAM
  - 32 Kbyte ROM
- Integrated LCD Controller
  - Up to 800 x 600 x 18-bit color
- Five UARTs
- I2S codec interface
- One high-speed USB 2.0 On-the-Go (OTG) controller and two USB 2.0 host interfaces
- Many general purpose I/O (GPIO) signals
- 32 independent DMA channels
- Programmable timers
- RTC
- Low power modes

See Freescale's *MCIMX31 Reference Manual* and *i.MX31 Data Sheet* for additional information. www.freescale.com/iMX

IMPORTANT NOTE: Please visit www.freescale.com/iMX for errata on the i.MX31.

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2.1.2 i.MX31 Microcontroller Block Diagram

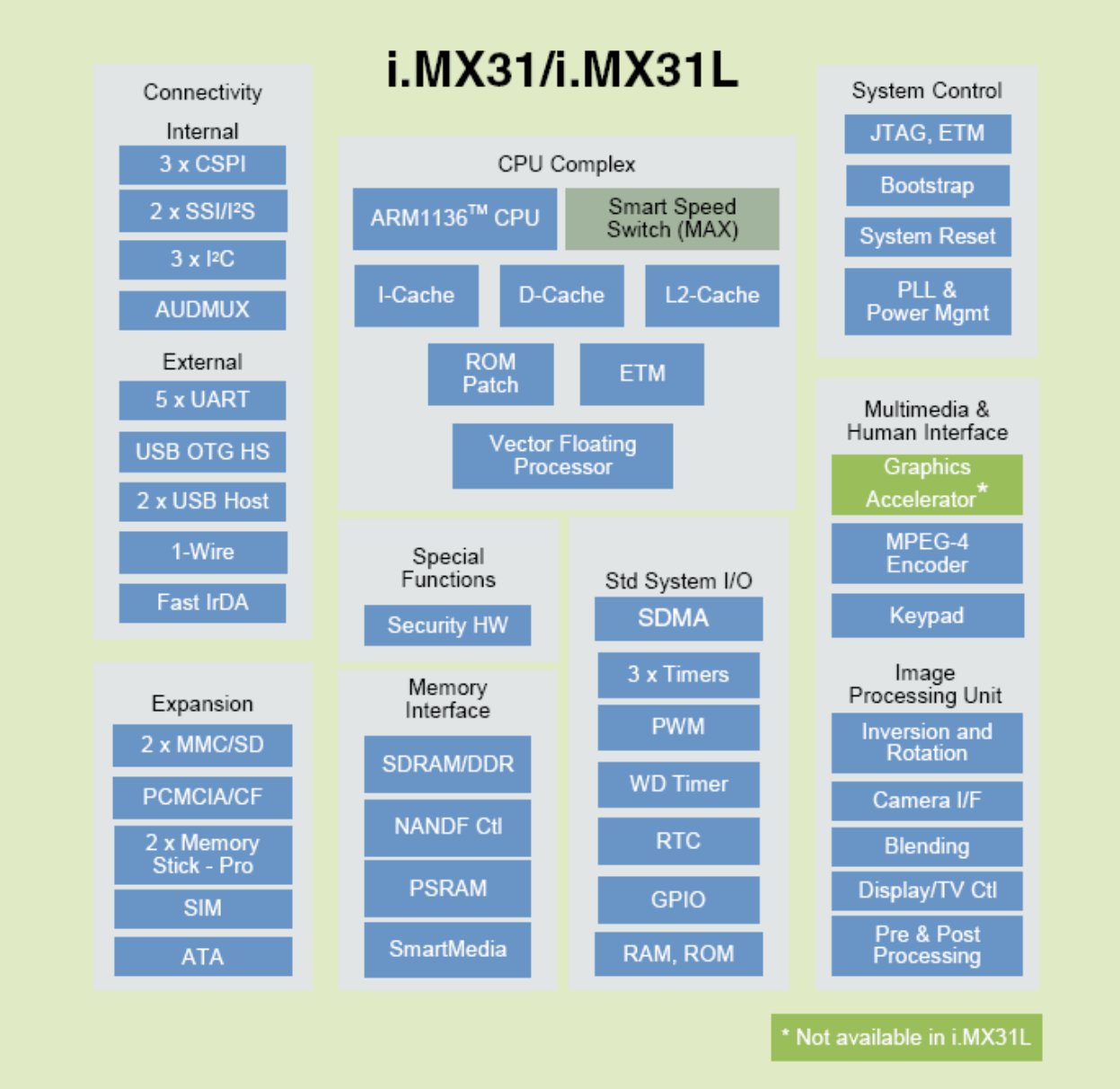

Figure 2.1: i.MX31 Microcontroller Block Diagram

2.2 Clocks

The i.MX31 requires an oscillator and crystal to enable proper internal timing. A 26.000 MHz oscillator is used to generate many of the processor's internal clocks via a series of PLLs and signal dividers. To generate the core CPU clock, the 26.000 MHz signal is run through a Digital PLL controlled by the Clock Controller Module (CCM) register. Divisors are used to divide down the internal bus frequency to set the LCD, memory controller, camera interface, etc.

IMPORTANT NOTE: Please see Freescale's *i.MX31 Reference Manual* for additional information about processor clocking.

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The second required crystal runs at 32.768 kHz. The 32.768 kHz clock is used for processor start up and as a reference clock for the Real Time Clock (RTC) Module.

The i.MX31's microcontroller core clock speed is initialized by software on the SOM-LV. The SDRAM bus speed is set at 133 MHz in LogicLoader. Other clock speeds, such as core speed and specific serial baud rates, can be supported and modified in software for specific user applications.

The i.MX31-10 SOM-LV provides an external bus clock, uP_BUS_CLK. The uP_BUS_CLK, which is connected to the processor's BCLK pin, is disabled by default. uP_SDCLK and uP_nSDCLK serve as the DDR RAM clocks on the i.MX31-10 SOM-LV.

i.MX31 Microcontroller Signal Name	i.MX31-10 SOM-LV Net Name	Default Software Value in LogicLoader
CORE	N/A	Up to 532 MHz
SDCLK	uP_SDCLK	133 MHz
SDCLK_B	uP_nSDCLK	133 MHz
BLCK	uP_BUS_CLK	Not configured

2.3 Memory

2.3.1 Low Power DDR Synchronous DRAM

The i.MX31-10 SOM-LV uses a 32-bit memory bus to interface to Low Power DDR SDRAM. The memory can be configured as 32, 64, 128, or 256 MBytes in order to meet the user's memory requirements and cost constraints. Logic's default memory configuration on the SOM-LV included in the Development Kit is specified as 128 MBytes.

2.3.2 Direct Memory Access (DMA)

The Freescale i.MX31 microcontroller has a direct memory access controller which contains multiple DMA channels (31) for use with internal peripherals to achieve highly efficient data throughput. For more information on using the DMA interface, please refer to the *i.MX31 Reference Manual*.

2.3.3 NOR Flash

The i.MX31-10 SOM-LV uses a 16-bit memory bus to interface to NOR flash memory chips. The onboard SOM-LV memory can be configured as 0, 2, or 4 MBytes to meet the user's flash requirements and cost constraints. Logic's default flash configuration is 2 MBytes on the SOM-LV included in the standard Development Kit. Because flash is one of the most expensive components on the i.MX31-10 SOM-LV, it is important to contact Logic when determining the necessary flash size for final product configuration. NAND flash is a lower cost alternative that should be considered for final product configuration.

It is possible to expand the system's non-volatile storage capability by adding external flash ICs, SD memory, CompactFlash®, or NAND flash. See the i.MX31-10 Development Kit for reference designs or contact Logic for other possible peripheral designs.

2.3.4 NAND Flash

The i.MX31-10 SOM-LV uses an 8-bit memory bus to interface to NAND flash. The product supports configurations of 16, 32, 64, 128 MBytes, and other sizes, depending on NAND

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availability. The SOM-LV included in the standard Development Kit contains 64 MBytes of NAND flash. Please contact Logic for more information.

2.3.5 PC Card Interface

The i.MX31-10 SOM-LV CPU directly supports a single PCMCIA or CompactFlash slot. The i.MX31-10 SOM-LV uses internal logic to provide the necessary signals for a PC card interface. The development kit reference design includes a hot-swappable CompactFlash connector. Additional CompactFlash slots can be added using the WEIM bus. Contact platformsupport@logicpd.com for more information on implementing additional slots.

2.4 10/100 Ethernet Controller

The i.MX31-10 SOM-LV uses an SMSC 9117 Ethernet controller to provide an easy-to-use networking interface. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. Logic provides an example circuit schematic in the i.MX31-10 Development Kit for reference. Please note the TX+/- and RX+/- pairs must be routed as differential pairs on the baseboard PCB.

2.5 Audio Codec

The i.MX31 processor has a Synchronous Serial Interface (SSI) controller that can support AC97 and I2S formats. This SSI controller implements a 5-pin serial interface to the I2S audio codec, in this case the Freescale MC13783. From the codec on the i.MX31-10 SOM-LV, the outputs are CODEC_OUTL and CODEC_OUTR. These signals are available from the expansion connectors.

The codec on the i.MX31 SOM-LV performs up to full-duplex codec functions and supports variable sample rates from 8k–96k samples per second.

NOTE: The Freescale i.MX31 SOM-LV also offers an SSI interface for other codec devices. This interface provides a digital interface that is multiplexed with the signals from the SSI controller. If you are looking for a different codec option, Logic has previously interfaced different high-performance audio codecs into other SOM-LVs. Contact Logic for assistance in selecting an appropriate audio codec for your application.

2.6 Display Interface

Freescale's i.MX31 microcontroller has a built in LCD controller supporting STN, color STN, HR-TFT, and TFT panels at up to 800 x 600 x 18-bit color resolution. See the *i.MX31 Reference Manual* for further information on the integrated LCD controller. The signals from the i.MX31's LCD controller are organized by bit and color and can be interfaced through the expansion connectors. Logic has written drivers for numerous panels of different types and sizes. Please contact Logic before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload.

2.7 Serial Interfaces

The i.MX31-10 SOM-LV comes with the following serial channels: UARTA, UARTB, UARTC, CSPI, and two I2C ports. If additional serial channels are required, please contact Logic for reference designs. Please see the *i.MX31 Reference Manual* for further information regarding serial communications.

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2.7.1 UARTA

UARTA has been configured to be the i.MX31-10 Development Kit's main serial port. It is an asynchronous 16C550-compatible UART. This UART provides a high-speed serial interface that uses First In / First Out (FIFO) and is capable of sending and receiving serial data simultaneously. The signals from the SOM-LV are Transistor-Transistor Logic (TTL) level signals, not RS232 level signals. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the Development Kit. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

UARTA's baud rate is set by default to 115.2 Kbits/s, though it supports most common serial baud rates.

2.7.2 UARTB

Serial Port UARTB is an asynchronous 16C550-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the SOM-LV are TTL level signals, not RS232 level signals. UARTB's baud rate can also be set to most common serial baud rates.

2.7.3 UARTC

Like UARTB, Serial Port UARTC is an asynchronous 16C550-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the SOM-LV are TTL level signals, not RS232 level signals. UARTC's baud rate can also be set to most common serial baud rates.

2.7.4 CSPI

The Configurable Serial Peripheral Interface (CSPI) is used on the SOM-LV to communicate with the onboard EEPROM and MC13783 codec. There are two chip selects available to the user. Please see the *i.MX31 Reference Manual* for further information.

2.7.5 I2C

The i.MX31-10 SOM-LV supports two external I2C ports. Both ports' clock and data signals have 2.2K pull-up resistors to their respective power rails. Please see the *i.MX31 Reference Manual* for further information.

2.8 USB Interface

The i.MX31 SOM-LV supports one USB 2.0 high-speed host port and one USB 2.0 On-the-Go (OTG) port which can function as a host or device/client. Both ports can operate at up to 480 Mb/s. The processor has the USB controller internal to the device for both the host and OTG port. The SOM-LV has external PHYs to support both interfaces.The PHYs are Philips ISP1504 devices. For more information on using both the USB host and OTG interfaces, please see the *i.MX31 Reference Manual*.

IMPORTANT NOTE: In order for USB to be correctly implemented on the i.MX31 SOM-LV, additional impedance matching circuitry may be required on the USBx_D+ and USBx_D- signals before they can be used. USB 2.0 requirements specify the signals must be routed as differential pairs with a 90 ohm differential impedance. Refer to the USB 2.0 specification for detailed information.

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2.9 ADC/Touch Interface

The i.MX31-10 SOM-LV uses the MC13783 integrated touch screen controller. The controller includes a 13-bit analog-to-digital converter (ADC). This TSC is used to support standard 4-wire resistive touch panels. The TSC has 6 A/D signals that are available externally off the connectors. The device is connected to the CPU by the CSPI interface. Please see the MC13783 Datasheet for more information.

2.10 General Purpose I/O

Logic designed the i.MX31-10 SOM-LV to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the SOM-LV that interface to the i.MX31. See the “Pin Descriptions” section of this hardware specification for more information. If certain peripherals are not desired, such as the LCD controller, chip selects, IRQs, or UARTS, then multiple GPIO pins become available. **Not all peripheral pins can be used as GPIOs**; verify your GPIO selection against Table 4-8 in the *i.MX31 Reference Manual*, available from Freescale's website.

2.11 Onboard Logic Interfaces

The onboard Logic interfaces are used to create additional functionality on the SOM-LV with the support of a few discrete logic components. The logic interface provides memory map selection between multiple chips as well as buffer direction and output control.

Memory Map

The onboard Logic creates a 2-area memory map from two CPU chip selects. When chip select 4 is asserted and A23 is low, onboard logic asserts the WRLAN_nCS signal, which is the onboard SMSC LAN9117 Ethernet chip enable. Asserting chip select 4 low and A23 high asserts the FAST_nCS signal, which goes off-board for customer use.

Chip Select	Offset	Device/Feature	Notes
nCS4	+ 0x00	WRLAN_nCS (Ethernet)	
nCS4	+ 0x00800000	FAST_nCS (customer use)	Offset is accurate when CS4 is setup for 16 bit accesses

2.12 Expansion/Feature Options

The i.MX31-10 SOM-LV was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user’s design. Some of these signals are buffered and brought out to the expansion connectors. It is possible for a user to expand the SOM-LV’s functionality even further by adding host bus or ISA bus devices. Some features that are implemented on the i.MX31, but are not discussed herein, include: RTC, pulse width modulation (PWM), Secure Digital, SIM card, SDIO cards, graphics accelerator, MPEG encoder, Image Processing Unit, 1wire interface, ATA interface, FIR, and the debug module. See the *i.MX31 Reference Manual* and the *i.MX31-10 SOM-LV Schematics* for more details. Logic has experience implementing additional options, including other audio codecs, Ethernet ICs, co-processors, and components on SOM-LV boards. Please contact Logic for potential reference designs before selecting your peripherals.

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3 System Integration

3.1 Configuration

The i.MX31-10 SOM-LV was designed to meet multiple applications for users with specific design and budget requirements. As a result, this SOM-LV supports a variety of embedded operating systems and supports the following hardware configurations:

- Flexible memory footprint: 64 or 128 MB Low Power DDR SDRAM
- Flexible NOR flash footprint: 0, 2, or 4 MB NOR flash
- Flexible NAND flash footprint: 0, 16, 32, 64 MB, or larger NAND flash
- Optional SMSC LAN9117 10/100 Ethernet controller

Please contact Logic for additional hardware configurations to meet your application needs.

3.2 Resets

The SOM-LV has a reset input (MSTR_nRST) and a reset output (RESET_nOUT). MSTR_nRST should be used by external devices to assert reset to the product. RESET_nOUT should be used to indicate to other devices that the SOM-LV is in reset.

3.2.1 Master Reset (MSTR_nRST)—Reset Input

Logic suggests that custom designs implemented with the i.MX31-10 SOM-LV use the MSTR_nRST signal as the “pin hole” reset used in commercial embedded systems. The MSTR_nRST triggers a power-on-reset event to the i.MX31 and resets the entire CPU.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition. (Powering-up in a low or bad power condition will cause data corruption and possible temporary system lockup). See the section entitled “Power Management” for further details. Either one of the following two conditions will cause a system-wide reset: power on the MSTR_nRST signal or a low pulse on the MSTR_nRST signal.

Low Pulse on MSTR_nRST Signal

A low pulse on the MSTR_nRST signal of the reset chip, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic suggests that for any external assertion source that triggers the MSTR_nRST signal, analog or digital, de-bouncing should be used to generate a clean, one-shot reset signal.

3.2.2 SOM-LV Reset (RESET_nOUT)—Reset output

All hardware peripherals should connect their hardware-reset pin to the RESET_nOUT signal on the expansion connector. Internally all SOM-LV peripheral hardware reset pins are connected to the RESET_nOUT net.

If the output of the onboard voltage-monitoring circuit is asserted (active low), the user can expect to lose information stored in RAM. The data loss occurs because the CPU is reset to its reset defaults.

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3.3 Booting from Internal or External Memory

The i.MX31 SOM-LV is configured by default to boot from onboard flash. To boot from external memory, tie EXT_BOOT_nSELECT to ground.

3.4 Interrupts

The i.MX31 incorporates the ARM1136JF-S Vectored Interrupt Controller (AVIC) which provides up to 64 interrupt sources to the ARM core. Refer to Freescale's *i.MX31 Reference Manual* for further information on using interrupts.

3.5 JTAG Debugger Interface

The JTAG connection on the i.MX31 allows recovery of corrupted flash memory and real-time application debug. When choosing a debugger product, remember that many different third-party JTAG debuggers are available for Freescale microcontrollers. The following signals make up the JTAG interface to the i.MX31: TDI, TMS, TCK, TDO, nTRST, RTCK, MSTR_nRST, and nDE. These signals should interface directly to a 20-pin 0.1" through-hole connector, as shown on the baseboard reference schematics.

IMPORTANT NOTE: When laying out the 20-pin connector, realize it may not be numbered as a standard 20-pin 0.1" insulation displacement connector (IDC) through-hole connector. See i.MX31-10 Development Kit reference design for further details. Each JTAG tool vendor may define the 20-pin IDC connector pin-out differently.

3.6 Power Management

3.6.1 System Power Supplies

In order to ensure a flexible design, the i.MX31-10 SOM-LV was designed to have the following power areas: MAIN_BATTERY, 5V, 3.3V_IN, 3.3V_uP_BATT. All power areas are inputs to the SOM-LV. The module also provides reference voltages to specific peripheral areas. Reference voltages are named VREF_xxxx on the expansion connectors, are outputs from the SOM-LV, and should be used as reference voltage inputs to level shifting devices on baseboard designs.

3.6.1.1 MAIN_BATTERY

The MAIN_BATTERY input is the main source of power for the SOM-LV. This input expects a voltage within typical single lithium-ion battery limits which generally operate from 2.7 V to 4.2 V. If a lithium-ion battery is not used as the main power source, it is recommended to supply a fixed 3.3 V supply. The MC13783 power management controller takes the MAIN_BATTERY rail input and creates all onboard voltages. If the design is required to maintain RAM contents in a critical power situation (e.g., low battery, loss of power), the MAIN_BATTERY supply should be maintained above the minimum level at all costs (see "Electrical Specification," Section 2). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and the processor is placed into the Standby state. (Please note the description of Standby mode in Section 3.5.3.3 below.) This supply must stay within the acceptable levels specified in Section 2 of this manual, "Electrical Specification," unless experiencing power down or critical power conditions.

Note: The MC13783 power management controller has the following default values for PUMS[3:1]:

Default value for PUMS3 = Open
Default value for PUMS2 = Ground

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Default value for PUMS1 = Open

3.6.1.2 5V

The charging circuitry is not populated on standard i.MX31 SOM-LVs; therefore, the 5V input needs to be tied to GND on the baseboard.

Note: If you have a custom i.MX31 SOM-LV that populates the charging circuitry, this 5V input should be supplied through a 5V supply on the baseboard. Custom configuration SOM-LVs are only available through the official Custom Module NPI Process. Please contact Logic Sales for more information about the Custom Module NPI Process: product.sales@logicpd.com.

3.6.1.3 3.3V_IN

The 3.3V_IN rail is used to power a few legacy devices on the SOM-LV which require 3.3 volts. The baseboard should provide 3.3V to the SOM-LV; typically, this is implemented as a low dropout (LDO) or switching regulator connected to the MAIN_BATTERY power source. This supply must stay within the acceptable levels specified in Section 2 of this manual, “Electrical Specification,” unless experiencing power down or critical power conditions. Under critical power conditions, Logic suggests notifying the system through the assertion of a Standby sequence first, and then powering this supply off.

3.6.1.4 3.3V_uP_BATT

This power rail is used to power the onboard Real Time Clock (RTC) and power management state machine internal to the MC13783 power management controller. This power rail should always be powered to maintain the clock and power state of the product. A lithium-ion coin cell typically supplies power to this rail. The MC13783 overrides this input when MAIN_BATTERY is applied.

3.6.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on the product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The i.MX31-10 SOM-LV was designed to keep these aspects in mind while providing maximum flexibility in software and system integration.

On the i.MX31 there are many different software configurations that drastically affect power consumption: microcontroller core clock frequency, bus clock frequency, peripheral clocks, bus modes, power management states (Run, Wait, Doze, State Retention, and Deep Sleep); peripheral power states and modes; product user scenarios; interrupt handling; and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. Information for these items can be found in the appropriate documents such as the *LogicLoader User’s Manual* or the specific BSP manual.

3.6.3 Microcontroller

The i.MX31 processor power management’s scheme was designed to be easy to use. There are five power management modes provided in the i.MX31 microcontroller: Run, Wait, Doze, State Retention, and Deep Sleep. Logic Product Development BSPs have simplified the power management scheme to three power states: Run, Suspend, and Standby. Please see the

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descriptions of all three states below, as well as Freescale's *i.MX31 Reference Manual*, for more details.

3.6.3.1 Run State

Run is the i.MX31 SOM-LV's normal operating state in which oscillator inputs and all clocks are hardware enabled. The i.MX31 can enter Run mode from any state. A Standby-to-Run transition occurs on any valid wakeup event, such as the assertion of MSTR_nRST or any enabled interrupt signal. All required power supplies are active in this state. Please see Freescale's *i.MX31 Reference Manual* for further information.

3.6.3.2 Suspend State

Suspend is the i.MX31 SOM-LV's hardware power-down state, allowing for lower power consumption. The Suspend state is designed to reduce power consumption while the i.MX31 is waiting for an event, such as a keyboard input. In Logic BSPs, the Suspend state is entered by asserting the nSUSPEND signal or through software. The Wait, Doze, or State Retention power state is entered. All power supplies remain active and system context is retained. An internal or external wakeup event can cause the processor to transition back to Run mode. Please see Freescale's *i.MX31 Reference Manual* for further information.

3.6.3.3 Standby State

Standby is the i.MX31 SOM-LV's lowest power state. This state is entered in Logic BSPs by asserting the nSTANDBY signal or through software. The i.MX31 processor is put into Stop state and all clocks are stopped. The MAIN_BATTERY power rail should be maintained if the Low Power DDR RAM contents wish to be retained. Internal or external wakeup events can cause a return to the Run state.

3.7 ESD Considerations

The i.MX31 SOM-LV was designed to interface to a customer's peripheral board, while remaining low cost and adaptable to many different applications. The SOM-LV does not provide any onboard ESD protection circuitry—this must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

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4 Memory & I/O Mapping

On the Freescale i.MX31 microcontroller, all address mapping for the Wireless External Interface Module (WEIM) and external chip selects is fixed. Please consult Freescale's *i.MX31 Reference Manual* for details.

DDR RAM and shared WEIM Bus

Mapped "Chip Select" signals for the FlexBus are available as outputs from the microcontroller and are assigned as follows:

i.MX31 Chip Select	CSCRxU	CSCRxL	CSCRxA	Off-board Signal Name	Notes
CS0	0x0000CF03	0xA0330D01	0x00220800	BOOT_nCS	Onboard NOR flash (0, 2, or 4 MB) or external boot device when EXT_BOOT_SELECT=0.
CS1	0x00000000	0x00000000	0x00000000	uP_nCS_A_EXT	Available for use by an off-board device as uP_nCS_A_EXT
CS2/CSD0	-	-	-	-	DDR RAM chip select 0 (64 or 128 MB)
CS3/CSD1	0x00000000	0x00000000	0x00000000	uP_nCS_B_EXT	Available for use by an off-board device as uP_nCS_B_EXT
CS4	0x00008701	0x04000541	0x00010000	FAST_nCS	Shared Area: LAN 9117 access when A23=0, off-board external use when A23=1 as FAST_nCS
CS5	0x00000000	0x00000000	0x00000000	SLOW_nCS	Available for use by an off-board device as SLOW_nCS

Chip select timings are based on the ARM AHB clock, also know as HCLK. For the i.MX31 SOM-LV, this clock is currently set to 133 MHz.

Please consult the *LogicLoader User's Manual* and the *LogicLoader User's Manual Addendum* for the i.MX31 SOM-LV for complete memory map information.

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5 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of LogicLoader (bootloader). Many of the signals defined in the tables below can be configured as input or outputs and have different functions. All GPIOs on the i.MX31 can be configured as either inputs or outputs, but not all pins can be configured as GPIOs (reference Table 4-8 in Freescale's *i.MX31 Reference Manual* for more details). It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull-ups/pull-downs).

5.1 J1 Connector 240-Pin Descriptions

J1 Pin#	Signal Name	I/O	Voltage	Description
1	RFU	I/O	NA	Reserved for future use. Do not connect.
2	RFU	I/O	NA	Reserved for future use. Do not connect.
3	RFU	I/O	NA	Reserved for future use. Do not connect.
4	RFU	I/O	NA	Reserved for future use. Do not connect.
5	RFU	I/O	NA	Reserved for future use. Do not connect.
6	RFU	I/O	NA	Reserved for future use. Do not connect.
7	RFU	I/O	NA	Reserved for future use. Do not connect.
8	RFU	I/O	NA	Reserved for future use. Do not connect.
9	RFU	I/O	NA	Reserved for future use. Do not connect.
10	RFU	I/O	NA	Reserved for future use. Do not connect.
11	DGND	I	GND	Ground. Connect to digital ground.
12	DGND	I	GND	Ground. Connect to digital ground.
13	uP_nWAKEUP	I	1.8V	Active low. Software can use this signal as an interrupt to transition to RUN state from lower power states. Software is required for proper operation. This signal has a 10K pull-up to 1.8V.
14	ETHER_TX+	O	3.3V	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-). Requires external magnetics. See example i.MX LITEKIT baseboard designs for reference components.
15	nSUSPEND	I	2.775V	Active low. Use this signal to enter and exit low power states from the run state. This signal remains powered and are pull up through a 10K resistor to a voltage (2.775V) internal to the SOM in all power states. Care should be taken to ensure that devices connected to these signals do not back power the internal rail through the 10K resistor. The signals should be driven low and floated to de-assert, a typical implementation is to connect one or more of these signals to a push button. Power management software is required to properly transition from the various power states.
16	ETHER_TX-	O	3.3V	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+). Requires external magnetics. See example i.MX LITEKIT baseboard designs for reference components.
17	nSTANDBY	I	2.775V	Active low. Use this signal to enter and exit low power states from the run state. This signal remains powered and are pull up through a 10K resistor to a voltage (2.775V) internal to the SOM in all power states. Care should be taken to ensure that devices connected to these signals do not back power the internal rail through the 10K resistor. The signals should be driven low and floated to de-assert, a typical implementation is to connect one or more of these signals to a push button. Power management software is required to properly transition from the various power states.

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J1 Pin#	Signal Name	I/O	Voltage	Description
18	ETHER_RX+	I	3.3V	This input pair receives 10/100 Mb/s Manchester-encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-). Requires external magnetics. See example i.MX LITEKIT baseboard designs for reference components.
19	USB1_ID	I/O	5.0V	Tie to pin four of a USB 2.0 OTG compliant connector. This signal negotiates host/device operation with an external USB product. See example i.MX LITEKIT baseboard designs for reference components.
20	ETHER_RX-	I	3.3V	This input pair receives 10/100 Mb/s Manchester-encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+). Requires external magnetics. See example i.MX LITEKIT baseboard designs for reference components.
21	USB1_VBUS	I	5.0V	Ties to pin one of a USB 2.0 OTG compliant connector. This signal indicates to the USB controller that an external USB Host has been connected as well as provides power to USB Device peripherals. See example i.MX LITEKIT baseboard designs for reference components.
22	LAN_LED2	O	3.3V	Active low. Asserts when there is valid Ethernet connection. Deasserts during Ethernet traffic indicating activity. See example i.MX LITEKIT baseboard designs for reference components.
23	USB1_nOC	I	3.3V	Active low. USB OTG over current flag. Indicates to PHY an over current condition exists on the USB OTG port.
24	LAN_LED1	O	3.3V	Active low. Asserts to indicate operation speed, either 10 Mb or 100 Mb connection. See example i.MX LITEKIT baseboard designs for reference components.
25	USB1_PWR_nEN	O	3.3V	Active low. USB OTG power enable. Enables power to the external USB power switch. See example i.MX LITEKIT baseboard designs for reference components.
26	VREF_ETHERNET	O	NA	AC coupled to GND. Output from the SOM-LV that drives the impedance network and magnetics. Specific to Ethernet PHY requirements. See example i.MX LITEKIT baseboard designs for reference components.
27	USB1_D+	I/O	3.3V	USB OTG port 1 I/O data plus signal. Route as differential pair with USB1_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
28	uP_AUX_CLK	O	1.8V	Processor's CLKO output.
29	USB1_D-	I/O	3.3V	USB OTG port 1 I/O data minus signal. Route as differential pair with USB1_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
30	PWR_ON	I	2.775V	Active high. Software can use this signal to enter RUN from low power modes. Software is required for correct operation. This signal has a 10K pull-up.
31	DGND	I	GND	Ground. Connect to digital ground.
32	DGND	I	GND	Ground. Connect to digital ground.
33	USB2_D+	I/O	3.3V	USB Host port 2 I/O data plus signal. Route as differential pair with USB2_D-. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
34	uP_GPIO_7	I/O	2.7V (NVCC6)	Processor GPIO available to user.
35	USB2_D-	I/O	3.3V	USB Host port 2 I/O data minus signal. Route as differential pair with USB2_D+. Follow USB 2.0 routing guidelines. Route pair with 90 ohms differential impedance.
36	uP_GPIO_6	I/O	2.7V (NVCC6)	Processor GPIO available to user.
37	USB2_nOC	I	3.3V	Active low. USB Host over current flag. Indicates to PHY an over current condition exists on the USB Host port.
38	uP_GPIO_5	I/O	2.7V (NVCC5)	Processor GPIO available to user.
39	USB2_PWR_nEN	O	3.3V	Active low. USB Host power enable. Enables power to the external USB power switch. See example i.MX LITEKIT baseboard designs for reference components.
40	uP_D0	I/O	1.8V	Processor Host bus (WEIM bus) data bit 0.
41	RFU	I/O	NA	Reserved for future use. Do not connect.

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J1 Pin#	Signal Name	I/O	Voltage	Description
42	uP_D1	I/O	1.8V	Processor Host bus (WEIM bus) data bit 1.
43	RFU	I/O	NA	Reserved for future use. Do not connect.
44	uP_D2	I/O	1.8V	Processor Host bus (WEIM bus) data bit 2.
45	RFU	I/O	NA	Reserved for future use. Do not connect.
46	uP_D3	I/O	1.8V	Processor Host bus (WEIM bus) data bit 3.
47	RFU	I/O	NA	Reserved for future use. Do not connect.
48	uP_D4	I/O	1.8V	Processor Host bus (WEIM bus) data bit 4.
49	3.3V_nEN	O	2.7V	3.3V external enable pin. Active low, signals to the baseboard the 3.3V supply should be enabled.
50	uP_D5	I/O	1.8V	Processor Host bus (WEIM bus) data bit 5.
51	DGND	I	GND	Ground. Connect to digital ground.
52	DGND	I	GND	Ground. Connect to digital ground.
53	A0 (DGND)	O	GND	Processor Host bus (WEIM bus) address bit 0. (see note 1 at the end of this table)
54	uP_D6	I/O	1.8V	Processor Host bus (WEIM bus) data bit 6.
55	A1 (uP_MA0)	O	1.8V	Processor Host bus (WEIM bus) address bit 1. (see note 1)
56	uP_D7	I/O	1.8V	Processor Host bus (WEIM bus) data bit 7.
57	A2 (uP_MA1)	O	1.8V	Processor Host bus (WEIM bus) address bit 2. (see note 1)
58	uP_D8	I/O	1.8V	Processor Host bus (WEIM bus) data bit 8.
59	A3 (uP_MA2)	O	1.8V	Processor Host bus (WEIM bus) address bit 3. (see note 1)
60	uP_D9	I/O	1.8V	Processor Host bus (WEIM bus) data bit 9.
61	A4 (uP_MA3)	O	1.8V	Processor Host bus (WEIM bus) address bit 4. (see note 1)
62	uP_D10	I/O	1.8V	Processor Host bus (WEIM bus) data bit 10.
63	A5 (uP_MA4)	O	1.8V	Processor Host bus (WEIM bus) address bit 5. (see note 1)
64	uP_D11	I/O	1.8V	Processor Host bus (WEIM bus) data bit 11.
65	A6 (uP_MA5)	O	1.8V	Processor Host bus (WEIM bus) address bit 6. (see note 1)
66	uP_D12	I/O	1.8V	Processor Host bus (WEIM bus) data bit 12.
67	A7 (uP_MA6)	O	1.8V	Processor Host bus (WEIM bus) address bit 7. (see note 1)
68	uP_D13	I/O	1.8V	Processor Host bus (WEIM bus) data bit 13.
69	A8 (uP_MA7)	O	1.8V	Processor Host bus (WEIM bus) address bit 8. (see note 1)
70	uP_D14	I/O	1.8V	Processor Host bus (WEIM bus) data bit 14.
71	DGND	I	GND	Ground. Connect to digital ground.
72	DGND	I	GND	Ground. Connect to digital ground.
73	A9 (uP_MA8)	O	1.8V	Processor Host bus (WEIM bus) address bit 9. (see note 1)
74	uP_D15	I/O	1.8V	Processor Host bus (WEIM bus) data bit 15.
75	A10 (uP_MA9)	O	1.8V	Processor Host bus (WEIM bus) address bit 10. (see note 1)
76	RFU	I/O	NA	Reserved for future use. Do not connect.
77	A11 (uP_MA10)	O	1.8V	Processor Host bus (WEIM bus) address bit 11. (see note 1)
78	RFU	I/O	NA	Reserved for future use. Do not connect.
79	A12 (uP_MA11)	O	1.8V	Processor Host bus (WEIM bus) address bit 12. (see note 1)
80	RFU	I/O	NA	Reserved for future use. Do not connect.
81	A13 (uP_MA12)	O	1.8V	Processor Host bus (WEIM bus) address bit 13. (see note 1)
82	RFU	I/O	NA	Reserved for future use. Do not connect.
83	A14 (uP_A13)	O	1.8V	Processor Host bus (WEIM bus) address bit 14. (see note 1)
84	RFU	I/O	NA	Reserved for future use. Do not connect.
85	A15 (uP_A14)	O	1.8V	Processor Host bus (WEIM bus) address bit 15. (see note 1)
86	RFU	I/O	NA	Reserved for future use. Do not connect.
87	A16 (uP_A15)	O	1.8V	Processor Host bus (WEIM bus) address bit 16. (see note 1)
88	RFU	I/O	NA	Reserved for future use. Do not connect.
89	A17 (uP_A16)	O	1.8V	Processor Host bus (WEIM bus) address bit 17. (see note 1)
90	RFU	I/O	NA	Reserved for future use. Do not connect.
91	DGND	I	GND	Ground. Connect to digital ground.
92	DGND	I	GND	Ground. Connect to digital ground.
93	A18 (uP_A17)	O	1.8V	Processor Host bus (WEIM bus) address bit 18. (see note 1)
94	RFU	I/O	NA	Reserved for future use. Do not connect.
95	A19 (uP_A18)	O	1.8V	Processor Host bus (WEIM bus) address bit 19. (see note 1)
96	RFU	I/O	NA	Reserved for future use. Do not connect.
97	A20 (uP_A19)	O	1.8V	Processor Host bus (WEIM bus) address bit 20. (see note 1)
98	RFU	I/O	NA	Reserved for future use. Do not connect.

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J1 Pin#	Signal Name	I/O	Voltage	Description
99	A21 (uP_A20)	O	1.8V	Processor Host bus (WEIM bus) address bit 21. (see note 1)
100	RFU	I/O	NA	Reserved for future use. Do not connect.
101	A22 (uP_A21)	O	1.8V	Processor Host bus (WEIM bus) address bit 22. (see note 1)
102	RFU	I/O	NA	Reserved for future use. Do not connect.
103	A23 (uP_A22)	O	1.8V	Processor Host bus (WEIM bus) address bit 23. (see note 1)
104	RFU	I/O	NA	Reserved for future use. Do not connect.
105	A24 (uP_A23)	O	1.8V	Processor Host bus (WEIM bus) address bit 24. (see note 1)
106	RFU	I/O	NA	Reserved for future use. Do not connect.
107	A25 (uP_A24)	O	1.8V	Processor Host bus (WEIM bus) address bit 25. (see note 1)
108	RFU	I/O	NA	Reserved for future use. Do not connect.
109	uP_nWAIT	I	1.8V	Active low. Processor Host bus (WIEM bus) ECB signal. Used to extend bus transactions beyond programmed wait states. The external device signals completion of the cycle by deasserting the uP_nWAIT signal. This signal has a 2.2K pull-up.
110	VREF_DATA_BUS	O	1.8V	Voltage reference output created on SOM-LV for the data bus.
111	DGND	I	GND	Ground. Connect to digital ground.
112	DGND	I	GND	Ground. Connect to digital ground.
113	uP_nIRQD	I	2.7V (NVCC8)	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.
114	CF_nCE (SLOW_nCS)	O	1.8V	Active low. Memory mode only CompactFlash chip enable. (see note 2)
115	uP_nIRQC	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.
116	CF_nWE (uP_nEB0)	O	1.8V	Active low. Memory mode CompactFlash write enable signal. Indicates the current SOM-LV bus transaction is writing data to the CompactFlash card. (see note 2)
117	uP_nIRQB	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.
118	CF_nOE (uP_nOE)	O	1.8V	Active low. Memory mode CompactFlash read enable signal. Indicates the current SOM-LV bus transaction is reading data from the CompactFlash card. (see note 2)
119	uP_nIRQA	I	1.8V	Active low. Software can use as a hardware interrupt. This signal is pulled high with a 10K resistor.
120	nCHRDY	I	3.3V	Active low. CompactFlash nCHRDY signal used to extend bus cycle to memory mode CompactFlash cards. This signal has a 470K pull-up to 3.3V. Note: baseboard should provide a pull up on nCHRDY to the voltage of the CompactFlash card being used. (see note 2)
121	BUFF_nOE_DATA	O	1.8V	Active low. When this signal is low, external devices can drive data onto the WEIM bus.
122	uP_UARTC_CTS	I	2.8V (NVCC3)	Clear To Send signal for CSPI3 UART.
123	BUFF_DIR_DATA	O	1.8V	When low, external buffers should drive data from external devices towards the SOM-LV. (SOM-LV is reading) When high, external buffers should drive data from the SOM-LV towards external devices. (SOM-LV is writing).
124	uP_UARTC_RTS	O	2.8V (NVCC3)	Ready To Send signal for CSPI3 UART.
125	uP_nOE	O	1.8V	Active low. Used to indicate processor is reading from external devices.
126	uP_UARTC_RX	I	2.8V (NVCC3)	Serial Data Receive signal for CSPI3 UART.
127	uP_RnW	O	1.8V	Low indicates processor is writing. High indicates processor is reading.
128	uP_UARTC_TX	O	2.8V (NVCC3)	Serial Data Transmit signal for CSPI3 UART.
129	DGND	I	GND	Ground. Connect to digital ground.
130	DGND	I	GND	Ground. Connect to digital ground.
131	uP_BUS_CLK	O	1.8V	Processor WEIM bus clock. Frequency varies based on software setup.
132	uP_UARTB_RX (IRDA_RX)	I	2.7V	Serial Data Receive signal for UART2.
133	uP_DREQ0	I	1.8V	External DMA request 0

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J1 Pin#	Signal Name	I/O	Voltage	Description
134	uP_UARTB_TX (IRDA_TX)	O	2.7V	Serial Data Transmit signal for UART2.
135	uP_DREQ1	I	1.8V	External DMA request 1
136	uP_UARTB_CTS	I	2.7V	Clear To Send signal for UART2.
137	uP_nBLE0 (uP_nEB0)	O	1.8V	Processor WEIM bus Byte Lane Enable 0 bits [7:0]
138	uP_UARTB_RTS	O	2.7V	Ready To Send signal for UART2.
139	uP_nBLE1 (uP_nEB1)	O	1.8V	Processor WEIM bus Byte Lane Enable 1 bits [15:8]
140	uP_GPIO_4	I/O	2.7V	Processor GPIO available to user.
141	uP_nCS_B_EXT	O	1.8V	External Chip select available for customer use.
142	uP_GPIO_3	I/O	2.7V	Processor GPIO available to user.
143	uP_nCS_A_EXT	O	1.8V	External Chip select available for customer use.
144	VREF_I2C1 (NVCC4)	O	2.8V (NVCC4)	Reference voltage output for I2C DATA and CLK signals
145	SLOW_nCS	O	1.8V	External Chip select available for customer use.
146	I2C1_DATA	I/O	2.8V (NVCC4)	I2C channel 1 data signal. This signal has a pull-up to the reference voltage onboard.
147	FAST_nCS	O	1.8V	External Chip select available for customer use.
148	I2C1_CLK	I/O	2.8V (NVCC4)	I2C channel 1 clock signal. This signal has a pull-up to the reference voltage onboard.
149	DGND	I	GND	Ground. Connect to digital ground.
150	DGND	I	GND	Ground. Connect to digital ground.
151	LCD_SPL	O	1.8V	LCD Start Pulse Left signal.
152	VREF_UARTA (2.7V_NVCC5/NVCC8)	O	2.7V	Voltage reference output for UART1 signals.
153	LCD_DON	O	1.8V	GPIO available for customer use.
154	uP_UARTA_DSR	O	2.7V	Data Set Ready signal for UART1.
155	LCD_CLS	O	1.8V	LCD CLS signal.
156	uP_UARTA_DTR	O	2.7V	Data Terminal Ready signal for UART1.
157	SPS (LCD_VSYNC/SPS)	O	1.8V	LCD SPS signal.
158	uP_UARTA_RX	I	2.7V	Data Receive signal for UART1.
159	HRLP (LCD_HSYNC/HRLP)	O	1.8V	LCD HRLP signal.
160	uP_UARTA_TX	O	2.7V	Data Transmit signal for UART1.
161	LCD_PANEL_PWR	O	1.8V	GPIO controlled by the LCD software to turn on the LCD panel before enabling the LCD controller.
162	uP_UARTA_CTS	I	2.7V	Clear To Send signal for UART1.
163	LCD_BACKLIGHT_PWR	O	1.8V	GPIO controlled by the LCD software to turn on the LCD backlight power before enabling the LCD controller.
164	uP_UARTA_RTS	O	2.7V	Ready To Send signal for UART1.
165	HSYNC (LCD_HSYNC/HRLP)	O	1.8V	LCD Horizontal Sync signal.
166	uP_GPIO_2	I/O	2.7V	Processor GPIO available to user.
167	VSYNC (LCD_VSYNC/SPS)	O	1.8V	LCD Vertical Sync Signal.
168	PWM0	O	2.8V (NVCC3)	PWM output 0.
169	DGND	I	GND	Ground. Connect to digital ground.
170	DGND	I	GND	Ground. Connect to digital ground.
171	LCD_DCLK	O	1.8V	LCD Data Clock output.
172	3.3V_uP_BATT	I	3.3V	External input that supplies power to the onboard power management controller and RTC interface. This signal should be powered by a coin-cell type battery or an always on power source.
173	LCD_REV	O	1.8V	LCD Reverse signal.
174	5V	I	5V	5V power input. **Note: The default population of the module does not include devices to support 5V power input or MAIN_BATTERY charging. If these options are desired, please contact sales@logicpd.com for information on obtaining a custom assembly.** With these custom options in place, the power management controller can use 5V to charge an external MAIN_BATTERY supply or power the SOM-LV. However, with the default population of the module, 5V should be grounded and power supplied through MAIN_BATTERY.

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J1 Pin#	Signal Name	I/O	Voltage	Description
175	LCD_MDISP (LCD_PSAVE/MDISP)	O	1.8V	TFT LCD data enable signal, driven by the LCD controller.
176	5V	I	5V	5V power input. **Note: The default population of the module does not include devices to support 5V power input or MAIN_BATTERY charging. If these options are desired, please contact sales@logicpd.com for information on obtaining a custom assembly.** With these custom options in place, the power management controller can use 5V to charge an external MAIN_BATTERY supply or power the SOM-LV. However, with the default population of the module, 5V should be grounded and power supplied through MAIN_BATTERY.
177	LCD_PSAVE (LCD_PSAVE/MDISP)	O	1.8V	LCD Power Save signal.
178	5V	I	5V	5V power input. **Note: The default population of the module does not include devices to support 5V power input or MAIN_BATTERY charging. If these options are desired, please contact sales@logicpd.com for information on obtaining a custom assembly.** With these custom options in place, the power management controller can use 5V to charge an external MAIN_BATTERY supply or power the SOM-LV. However, with the default population of the module, 5V should be grounded and power supplied through MAIN_BATTERY.
179	RFU	I/O	NA	Reserved for future use. Do not connect.
180	3.3V_IN	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.
181	RFU	I/O	NA	Reserved for future use. Do not connect.
182	3.3V_IN	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.
183	VREF_LCD (1.8V_NVCC7)	O	1.8V	Voltage reference output for the LCD interface.
184	3.3V_IN	I	3.3V	External 3.3V power input. This signal supplies power to 3.3V components onboard.
185	R1 (LD13)	O	1.8V	LCD R1 data bit when operating in 16 bpp 5:6:5 color mode.
186	TOUCH_LEFT	I	max 2.7V	Touch panel LEFT input signal.
187	R2 (LD14)	O	1.8V	LCD R2 data bit when operating in 16 bpp 5:6:5 color mode.
188	TOUCH_RIGHT	I	max 2.7V	Touch panel RIGHT input signal.
189	DGND	I	GND	Ground. Connect to digital ground.
190	DGND	I	GND	Ground. Connect to digital ground.
191	R3 (LD15)	O	1.8V	LCD R3 data bit when operating in 16 bpp 5:6:5 color mode.
192	TOUCH_BOTTOM	I	max 2.7V	Touch panel BOTTOM input signal.
193	R4 (LD16)	O	1.8V	LCD R4 data bit when operating in 16 bpp 5:6:5 color mode.
194	TOUCH_TOP	I	max 2.7V	Touch panel TOP input signal.
195	R5 (LD17)	O	1.8V	LCD R5 data bit when operating in 16 bpp 5:6:5 color mode.
196	A/D4	I	max 2.7V	Analog to digital converter input 4.
197	G0 (LD6)	O	1.8V	LCD G0 data bit when operating in 16 bpp 5:6:5 color mode.
198	A/D3	I	max 2.7V	Analog to digital converter input 3.
199	G1 (LD7)	O	1.8V	LCD G1 data bit when operating in 16 bpp 5:6:5 color mode.
200	A/D2	I	max 2.7V	Analog to digital converter input 2.
201	G2 (LD8)	O	1.8V	LCD G2 data bit when operating in 16 bpp 5:6:5 color mode.
202	A/D1	I	max 2.7V	Analog to digital converter input 1.
203	G3 (LD9)	O	1.8V	LCD G3 data bit when operating in 16 bpp 5:6:5 color mode.
204	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
205	G4 (LD10)	O	1.8V	LCD G4 data bit when operating in 16 bpp 5:6:5 color mode.
206	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
207	G5 (LD11)	O	1.8V	LCD G5 data bit when operating in 16 bpp 5:6:5 color mode.

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J1 Pin#	Signal Name	I/O	Voltage	Description
208	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
209	DGND	I	GND	Ground. Connect to digital ground.
210	DGND	I	GND	Ground. Connect to digital ground.
211	B1 (LD1)	O	1.8V	LCD B1 data bit when operating in 16 bpp 5:6:5 color mode.
212	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
213	B2 (LD2)	O	1.8V	LCD B2 data bit when operating in 16 bpp 5:6:5 color mode.
214	MAIN_BATTERY	I	max 4.6V	External power source input. This signal should be driven directly by a single cell lithium-ion battery or a fixed 3.3V regulated power source.
215	B3 (LD3)	O	1.8V	LCD B3 data bit when operating in 16 bpp 5:6:5 color mode.
216	uP_GPIO_1	I/O	1.8V	Processor GPIO available to user.
217	B4 (LD4)	O	1.8V	LCD B4 data bit when operating in 16 bpp 5:6:5 color mode.
218	uP_GPIO_0	I/O	1.8V	Processor GPIO available to user.
219	B5 (LD5)	O	1.8V	LCD B5 data bit when operating in 16 bpp 5:6:5 color mode.
220	uP_SPI_CS1	O	1.8V	SPI interface chip select 1 output.
221	ONE_WIRE (BATT_LINE)	I/O	2.7V	Bi-directional battery management ONEWIRE interface.
222	uP_SPI_CS0	O	1.8V	SPI interface chip select 0 output.
223	uP_SW_nRESET	I	2.7V	Active low. Input to CPU. Software can setup GPIO as an interrupt. Signal has a 10K pull-up to 2.7V.
224	uP_SPI_RX	I	1.8V	SPI interface receive input.
225	RESET_nOUT (PMIC_nRESET)	O	1.8V	Active low. Reset output from the power management controller that drives all onboard reset inputs. This signal should be used to drive reset inputs on external chips that require similar timing to the onboard devices. The RESET_nOUT signal has an onboard 4.7K pull-up to 1.8V_NVCC1 rail.
226	uP_SPI_TX	O	1.8V	SPI interface transmit output.
227	MSTR_nRST	I	1.8V	Active low. External reset input to the SOM-LV. This signal should be used to reset all devices on the SOM-LV including the CPU. The MSTR_nRST signal has an onboard 4.7K pull-up to 1.8V_NVCC1 rail.
228	uP_SPI_SCLK	I/O	1.8V	SPI Serial clock signal.
229	DGND	I	GND	Ground. Connect to digital ground.
230	DGND	I	GND	Ground. Connect to digital ground.
231	RFU	I/O	NA	Reserved for future use. Do not connect.
232	RFU	I/O	NA	Reserved for future use. Do not connect.
233	RFU	I/O	NA	Reserved for future use. Do not connect.
234	RFU	I/O	NA	Reserved for future use. Do not connect.
235	RFU	I/O	NA	Reserved for future use. Do not connect.
236	RFU	I/O	NA	Reserved for future use. Do not connect.
237	RFU	I/O	NA	Reserved for future use. Do not connect.
238	RFU	I/O	NA	Reserved for future use. Do not connect.
239	RFU	I/O	NA	Reserved for future use. Do not connect.
240	RFU	I/O	NA	Reserved for future use. Do not connect.

Note 1: The signals in parentheses are the net names specific to i.MX31-10 SOM-LV; the non-parenenthetical names are the signal names that are general to the form factor module.

Note 2: CF_nCE, CF_nOE, and CF_nWE can be used as control signals with WEIM Address and Data to create an external memory mode only CompactFlash interface. These signals are not used for the standard CompactFlash / PC card interface that is available on J2, nor are they used for the J4 CompactFlash socket available on the LV-Baseboard.

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5.2 J2 Connector 240-Pin Descriptions

J2 Pin#	Signal Name	I/O	Voltage	Description
1	RFU	I/O	NA	Reserved for future use. Do not connect.
2	RFU	I/O	NA	Reserved for future use. Do not connect.
3	RFU	I/O	NA	Reserved for future use. Do not connect.
4	RFU	I/O	NA	Reserved for future use. Do not connect.
5	RFU	I/O	NA	Reserved for future use. Do not connect.
6	RFU	I/O	NA	Reserved for future use. Do not connect.
7	RFU	I/O	NA	Reserved for future use. Do not connect.
8	RFU	I/O	NA	Reserved for future use. Do not connect.
9	RFU	I/O	NA	Reserved for future use. Do not connect.
10	RFU	I/O	NA	Reserved for future use. Do not connect.
11	DGND	I	GND	Ground. Connect to digital ground.
12	DGND	I	GND	Ground. Connect to digital ground.
13	PCC_POWER_nEN	O	1.8V	Active low. Turns on power to CompactFlash/PC Card interface.
14	PCC_nOE (uP_nLBA)	O	1.8V	Active low. CompactFlash/PC Card per transaction bus buffer Output Enable signal.
15	PCC_PCMCIA_nEN	O	1.8V	Active low. Enables CompactFlash address and control signals.
16	uP_PCC_RDYA	I	2.8V (NVCC3)	Active high. CompactFlash/PC Card Ready signal.
17	RFU	I/O	NA	Reserved for future use. Do not connect.
18	uP_PCC_nWAIT	I	2.8V (NVCC3)	Active low. CompactFlash/PC Card Wait signal.
19	RFU	I/O	NA	Reserved for future use. Do not connect.
20	uP_PCC_BVD2	I	2.8V (NVCC3)	CompactFlash/PC Card Battery Voltage Detect 2 input.
21	ATA_D15 (I2C1_DATA)	I/O	2.8V (NVCC4)	ATA interface Data bit 15. This interface is multiplexed with other onboard interfaces.
22	uP_PCC_BVD1	I	2.8V (NVCC3)	CompactFlash/PC Card Battery Voltage Detect 1 input.
23	ATA_D14 (I2C1_CLK)	I/O	2.8V (NVCC4)	ATA interface Data bit 14. This interface is multiplexed with other onboard interfaces.
24	uP_PCC_CD2	I	2.8V (NVCC3)	CompactFlash/ PC Card Detect 2 input.
25	ATA_D13 (CSI_PCLK)	I/O	2.8V (NVCC4)	ATA interface Data bit 13. This interface is multiplexed with other onboard interfaces.
26	uP_PCC_CD1	I	2.8V (NVCC3)	CompactFlash/ PC Card Detect 1 input.
27	ATA_D12 (CSI_HSYNC)	I/O	2.8V (NVCC4)	ATA interface Data bit 12. This interface is multiplexed with other onboard interfaces.
28	uP_PCC_VS1	I	2.8V (NVCC3)	CompactFlash/ PC Card Voltage Sense 1 input.
29	ATA_D11 (CSI_VSYNC)	I/O	2.8V (NVCC4)	ATA interface Data bit 11. This interface is multiplexed with other onboard interfaces.
30	uP_PCC_VS2	I	2.8V (NVCC3)	CompactFlash/PC Card Voltage Sense 2 input.
31	DGND	I	GND	Ground. Connect to digital ground.
32	DGND	I	GND	Ground. Connect to digital ground.
33	ATA_D10 (CSI_MCLK)	I/O	2.8V (NVCC4)	ATA interface Data bit 10. This interface is multiplexed with other onboard interfaces.
34	uP_PCC_RESET	O	2.8V (NVCC3)	CompactFlash/PC Card Reset output.
35	ATA_D9 (CSI_D15)	I/O	2.8V (NVCC4)	ATA interface Data bit 9. This interface is multiplexed with other onboard interfaces.
36	PCC_nDRV (uP_PC_POE)	O	2.8V (NVCC3)	CompactFlash/PC Card buffer Drive output.
37	ATA_D8 (CSI_D14)	I/O	2.8V (NVCC4)	ATA interface Data bit 8. This interface is multiplexed with other onboard interfaces.
38	PCC_nIOWR (uP_nOE)	O	1.8V	Active low. CompactFlash/PC Card I/O Write output.
39	ATA_D7 (CSI_D13)	I/O	2.8V (NVCC4)	ATA interface Data bit 7. This interface is multiplexed with other onboard interfaces.
40	PCC_nWE (uP_RnW)	O	1.8V	Active low. CompactFlash/PC Card Write Enable output.
41	ATA_D6 (CSI_D12)	I/O	2.8V (NVCC4)	ATA interface Data bit 6. This interface is multiplexed with other onboard interfaces.

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J2 Pin#	Signal Name	I/O	Voltage	Description
42	PCC_nIORD (uP_nEB1)	O	1.8V	Active low. CompactFlash/PC Card I/O Read output.
43	ATA_D5 (CSI_D11)	I/O	2.8V (NVCC4)	ATA interface Data bit 5. This interface is multiplexed with other onboard interfaces.
44	PCC_REG (uP_nEB0)	O	1.8V	CompactFlash/PC Card Reg access output.
45	ATA_D4 (CSI_D10)	I/O	2.8V (NVCC4)	ATA interface Data bit 4. This interface is multiplexed with other onboard interfaces.
46	uP_PCC_nIOIS16	I	2.8V (NVCC3)	CompactFlash/PC Card nIOIS16 input.
47	ATA_D3 (CSI_D9)	I/O	2.8V (NVCC4)	ATA interface Data bit 3. This interface is multiplexed with other onboard interfaces.
48	PCC_nCE1A (uP_MSDBA1)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 1A.
49	ATA_D2 (CSI_D8)	I/O	2.8V (NVCC4)	ATA interface Data bit 2. This interface is multiplexed with other onboard interfaces.
50	PCC_nCE2A (uP_MSDBA0)	O	1.8V	Active low. CompactFlash/PC Card Chip Enable 2A.
51	DGND	I	GND	Ground. Connect to digital ground.
52	DGND	I	GND	Ground. Connect to digital ground.
53	ATA_D1 (CSI_D7)	I/O	2.8V (NVCC4)	ATA interface Data bit 1. This interface is multiplexed with other onboard interfaces.
54	VREF_PCMCIA (NVCC3)	O	2.8V (NVCC3)	CompactFlash/PC Card Voltage reference output.
55	ATA_D0 (CSI_D6)	I/O	2.8V (NVCC4)	ATA interface Data bit 0. This interface is multiplexed with other onboard interfaces.
56	MFP (uP_A25)	O	1.8V	Processor WEIM bus Address bit 25 output.
57	IORDY (PWMO)	O	2.8V (NVCC3)	ATA interface IORDY output. This interface is multiplexed with other onboard interfaces.
58	RFU	I/O	NA	Reserved for future use. Do not connect.
59	ATA_RESET	O	2.8V (NVCC3)	ATA interface Reset output. This interface is multiplexed with other onboard interfaces.
60	RFU	I/O	NA	Reserved for future use. Do not connect.
61	ATA_DMACK	O	2.8V (NVCC3)	ATA interface DMA Acknowledge output. This interface is multiplexed with other onboard interfaces.
62	RFU	I/O	NA	Reserved for future use. Do not connect.
63	ATA_DIOW (CSI_D3)	O	2.8V (NVCC3)	ATA interface Data I/O Write output. This interface is multiplexed with other onboard interfaces.
64	RFU	I/O	NA	Reserved for future use. Do not connect.
65	ATA_DIOR (CSI_D2)	O	2.8V (NVCC3)	ATA interface Data I/O Read output. This interface is multiplexed with other onboard interfaces.
66	RFU	I/O	NA	Reserved for future use. Do not connect.
67	ATA_CS1 (CSI_D1)	O	2.8V (NVCC3)	ATA interface Chip Select 1 output. This interface is multiplexed with other onboard interfaces.
68	RFU	I/O	NA	Reserved for future use. Do not connect.
69	ATA_CS0 (CSI_D0)	O	2.8V (NVCC3)	ATA interface Chip Select 0 output. This interface is multiplexed with other onboard interfaces.
70	RFU	I/O	NA	Reserved for future use. Do not connect.
71	DGND	I	GND	Ground. Connect to digital ground.
72	DGND	I	GND	Ground. Connect to digital ground.
73	RFU	I/O	NA	Reserved for future use. Do not connect.
74	RFU	I/O	NA	Reserved for future use. Do not connect.
75	RFU	I/O	NA	Reserved for future use. Do not connect.
76	RFU	I/O	NA	Reserved for future use. Do not connect.
77	RFU	I/O	NA	Reserved for future use. Do not connect.
78	RFU	I/O	NA	Reserved for future use. Do not connect.
79	RFU	I/O	NA	Reserved for future use. Do not connect.
80	VREF_MMC/SD1 (NVCC3)	O	2.8V (NVCC3)	MMC/SD1 interface voltage reference output.
81	CDCOUT	O	2.7V	MC13783 CDCOUT signal.
82	SD1_DATA3	I/O	2.8V (NVCC3)	MMC/SD1 Data 3 signal.
83	uP_CSPI1_RDY	I	1.8V_NVCC10	CSPI1 Ready signal.
84	SD1_DATA2	I/O	2.8V (NVCC3)	MMC/SD1 Data 2 signal.
85	uP_CSPI2_RDY	I	2.7V_NVCC5,8	CSPI2 Ready signal.
86	SD1_DATA1	I/O	2.8V (NVCC3)	MMC/SD1 Data 1 signal.
87	uP_CSPI2_SS2	O	2.7V_NVCC5,8	CSPI2 Slave Select 2 signal.

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J2 Pin#	Signal Name	I/O	Voltage	Description
88	SD1_DATA0	I/O	2.8V (NVCC3)	MMC/SD1 Data 0 signal.
89	uP_CSPI2_SS1	O	2.7V_NVCC5,8	CSPI2 Slave Select 1 signal.
90	SD1_CMD	I/O	2.8V (NVCC3)	MMC/SD1 Command signal.
91	DGND	I	GND	Ground. Connect to digital ground.
92	DGND	I	GND	Ground. Connect to digital ground.
93	PCC_PCMCIA_nEN	O	1.8	Active low. Enables CompactFlash address and control signals.
94	SD1_CLK	I/O	2.8V (NVCC3)	MMC/SD1 Clock signal.
95	KEY_COL6	I/O	2.7V_NVCC6,9	Keypad Column 6 signal.
96	VREF_I2C2 (2.7V_NVCC5/NVCC8)	O	2.7V_NVCC5,8	I2C channel 2 voltage reference output.
97	KEY_COL5	I/O	2.7V_NVCC6,9	Keypad Column 5 signal.
98	I2C2_CLK	I/O	2.7V_NVCC5,8	I2C channel 2 Clock signal.
99	KEY_COL4	I/O	2.7V_NVCC6,9	Keypad Column 4 signal.
100	I2C2_DATA	I/O	2.7V_NVCC5,8	I2C channel 2 Data signal.
101	KEY_COL3	I/O	2.7V_NVCC6,9	Keypad Column 3 signal.
102	uP_TEST1	I	2.7V_NVCC6,9	Test 1 signal tied to CPU SJC_MOD signal to enable / disable JTAG access. This signal has a 4.7k ohm pull down.
103	KEY_COL2	I/O	2.7V_NVCC6,9	Keypad Column 2 signal.
104	uP_TEST2	I	2.7V_NVCC5,8	Test 2 signal tied to CPU CE_CONTROL signal. Refer to MX31 documentation for more information on this signal. This signal has a 1k ohm pull down.
105	KEY_COL1	I/O	2.7V_NVCC6,9	Keypad Column 1 signal.
106	uP_DE	I	2.7V_NVCC6,9	CPU JTAG Debug Request signal. This signal has a 4.7k ohm pull up.
107	KEY_COL0	I/O	2.7V_NVCC6,9	Keypad Column 0 signal.
108	uP_TMS	I	2.7V_NVCC6,9	CPU JTAG Test Mode Signal. This signal has a 4.7k ohm pull up.
109	KEY_ROW7	I/O	2.7V_NVCC6,9	Keypad Row 7 signal.
110	uP_TCK	I	2.7V_NVCC6,9	CPU JTAG Test Clock input signal.
111	DGND	I	GND	Ground. Connect to digital ground.
112	DGND	I	GND	Ground. Connect to digital ground.
113	KEY_ROW6	I/O	2.7V_NVCC6,9	Keypad Row 6 signal.
114	uP_TDO	O	2.7V_NVCC6,9	CPU JTAG Test Data Output from the CPU to the JTAG device.
115	uP_GPIO_7	I/O	2.7V_NVCC6,9	Keypad Row 5 signal.
116	uP_nTRST	I	2.7V_NVCC6,9	CPU JTAG Test Reset input. This signal has a 4.7k ohm pull up.
117	uP_GPIO_6	I/O	2.7V_NVCC6,9	Keypad Row 4 signal.
118	uP_TDI	I	2.7V_NVCC6,9	CPU JTAG Test Data Input to the CPU from the JTAG device. This signal has a 4.7k ohm pull-up.
119	KEY_ROW3	I/O	2.7V_NVCC6,9	Keypad Row 3 signal.
120	uP_RTCK	O	2.7V_NVCC6,9	CPU JTAG Return Test Clock signal.
121	KEY_ROW2	I/O	2.7V_NVCC6,9	Keypad Row 2 signal.
122	VREF_JTAG (2.7V_NVCC6/NVCC9)	O	2.7V_NVCC6,9	CPU JTAG reference voltage output.
123	KEY_ROW1	I/O	2.7V_NVCC6,9	Keypad Row 1 signal.
124	SIM0_VEN	O	2.7V_NVCC6,9	SIM Card 0 Voltage Enable signal.
125	KEY_ROW0	I/O	2.7V_NVCC6,9	Keypad Row 0 signal.
126	SIM0_nDETECT	I	2.7V_NVCC6,9	Sim Card 0 Insertion Detect signal.
127	CSI_HSYNC	I/O	2.8V (NVCC4)	Camera Sensor Interface Horizontal Sync signal.
128	SIM0_CLK	I/O	2.7V_NVCC6,9	SIM Card 0 Clock signal.
129	DGND	I	GND	Ground. Connect to digital ground.
130	DGND	I	GND	Ground. Connect to digital ground.
131	CSI_VSYNC	I/O	2.8V (NVCC4)	Camera Sensor Interface Vertical Sync signal.
132	SIM0_IO/TX	I/O	2.7V_NVCC6,9	SIM Card 0 I/O Transmit signal.
133	CSI_D0	I/O	2.8V (NVCC3)	Camera Sensor Interface Data bit 0.
134	SIM0_RX	I/O	2.7V_NVCC6,9	SIM Card 0 Receive signal.
135	CSI_D1	I/O	2.8V (NVCC3)	Camera Sensor Interface Data bit 1.
136	SIM0_nRESET	I/O	2.7V_NVCC6,9	SIM Card 0 Reset signal. Active low.
137	CSI_D2	I/O	2.8V (NVCC3)	Camera Sensor Interface Data bit 2.

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J2 Pin#	Signal Name	I/O	Voltage	Description
138	SIM0_VCC	O	SIM0_VCC	SIM Card 0 Voltage Output signal.
139	CSI_D3	I/O	2.8V (NVCC3)	Camera Sensor Interface Data bit 3.
140	RFU	I/O	NA	Reserved for future use. Do not connect.
141	CSI_D4	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 4.
142	RFU	I/O	NA	Reserved for future use. Do not connect.
143	CSI_D5	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 5.
144	RFU	I/O	NA	Reserved for future use. Do not connect.
145	CSI_D6	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 6.
146	RFU	I/O	NA	Reserved for future use. Do not connect.
147	CSI_D7	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 7.
148	RFU	I/O	NA	Reserved for future use. Do not connect.
149	DGND	I	GND	Ground. Connect to digital ground.
150	DGND	I	GND	Ground. Connect to digital ground.
151	CSI_D8	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 8.
152	PCC_POWER_nEN	O	1.8V_NVCC7	When asserted low this signal should turn power on to CompactFlash/ CF Card slot.
153	CSI_D9	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 9.
154	LCD_LCS0	O	1.8V_NVCC7	LCD Chip Select 0 signal.
155	CSI_D10	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 10.
156	LCD_CONTRAST	O	1.8V_NVCC7	LCD Contrast signal.
157	CSI_D11	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 11.
158	LCD_WRITE	O	1.8V_NVCC7	LCD Write Enable signal.
159	CSI_D12	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 12.
160	LCD_READ	O	1.8V_NVCC7	LCD Read Enable signal.
161	CSI_D13	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 13.
162	LCD_VSYNC0	O	1.8V_NVCC7	LCD Vertical Sync 0 signal.
163	CSI_D14	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 14.
164	LCD_PAR_RS	O	1.8V_NVCC7	LCD Parallel RS signal.
165	CSI_D15	I/O	2.8V (NVCC4)	Camera Sensor Interface Data bit 15.
166	LCD_SER_RS	O	1.8V_NVCC7	LCD Serial RS signal.
167	CSI_MCLK	I/O	2.8V (NVCC4)	Camera Sensor Interface Master Clock signal.
168	EXT_BOOT_nSELECT	I	1.8V	Boot select signal (0 = external boot device, 1 = onboard flash). This is accomplished by onboard logic: if signal EXT_BOOT_nSELECT is high, then FLASH_nCS = uP_nCS0; if signal EXT_BOOT_nSELECT is low, then BOOT_nCS = uP_nCS0. This defaults to the onboard flash if left unconnected (pulled to 1.8V through a 10K resistor).
169	DGND	I	GND	Ground. Connect to digital ground.
170	DGND	I	GND	Ground. Connect to digital ground.
171	CSI_PCLK	I/O	2.8V (NVCC4)	Camera Sensor Interface Pixel Clock signal.
172	BOOT_nCS	O	1.8V	Active Low. This signal is the chip select for boot ROM in area 0 when EXT_BOOT_nSELECT is low. When EXT_BOOT_nSELECT is high, this signal is inactive. See memory map for addressing details.
173	VREF_CSI (NVCC4)	O	2.8V (NVCC4)	Camera Sensor Interface reference voltage output.
174	RFU	I/O	NA	Reserved for future use. Do not connect.
175	LEDB3	O	max 5.5V	LED Drive Blue bit 3.
176	RFU	I/O	NA	Reserved for future use. Do not connect.
177	LEDG3	O	max 5.5V	LED Drive Green bit 3.
178	RFU	I/O	NA	Reserved for future use. Do not connect.
179	LEDR3	O	max 5.5V	LED Drive Red bit 3.
180	RFU	I/O	NA	Reserved for future use. Do not connect.
181	LEDB2	O	max 5.5V	LED Drive Blue bit 2.
182	B0 (LD0)	O	1.8V_NVCC7	LCD B0 data bit.
183	LEDG2	O	max 5.5V	LED Drive Green bit 2.
184	RFU	I/O	NA	Reserved for future use. Do not connect.
185	LEDR2	O	max 5.5V	LED Drive Red bit 2.
186	RFU	I/O	NA	Reserved for future use. Do not connect.
187	LEDB1	O	max 5.5V	LED Drive Blue bit 1.

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J2 Pin#	Signal Name	I/O	Voltage	Description
188	R0 (LD12)	O	1.8V_NVCC7	RLCD R0 data bit.
189	DGND	I	GND	Ground. Connect to digital ground.
190	DGND	I	GND	Ground. Connect to digital ground.
191	LEDG1	O	max 5.5V	LED Drive Green bit 1.
192	HSPGF	O	2.7V	See MC13783 data sheet for more information.
193	LEDR1	O	max 5.5V	LED Drive Red bit 1.
194	HSPGS	O	2.7V	See MC13783 data sheet for more information.
195	LEDKP	O	max 5.5V	LED Key Press signal.
196	LSPL	O	2.7V	See MC13783 data sheet for more information.
197	LEDAD2	O	max 5.5V	LED AD2 signal.
198	SPM	O	2.7V	See MC13783 data sheet for more information.
199	LEDAD1	O	max 5.5V	LED AD1 signal.
200	SPP	O	2.7V	See MC13783 data sheet for more information.
201	LEDMD4	O	max 5.5V	LED MD4 signal.
202	LSPM	O	2.7V	See MC13783 data sheet for more information.
203	LEDMD3	O	max 5.5V	LED MD3 signal.
204	LSPP	O	2.7V	See MC13783 data sheet for more information.
205	LEDMD2	O	max 5.5V	LED MD2 signal.
206	A/D6	I	max 2.7V	Analog to Digital Converter 6 input.
207	LEDMD1	O	max 5.5V	LED MD1 signal.
208	A/D5	I	max 2.7V	Analog to Digital Converter 5 input.
209	DGND	I	GND	Ground. Connect to digital ground.
210	DGND	I	GND	Ground. Connect to digital ground.
211	HSLDET	I	2.7V	Head Set Left detect signal.
212	MIC_IN	I	2.7V	Microphone input.
213	PC_PWRON	O	2.8V (NVCC3)	PC Card power applied input.
214	MIC_INR	I	2.7V	Right side microphone input.
215	ATLAS_GPO3	O	2.7V	MC13783 general purpose output.
216	MIC_INL	I	2.7V	Left side microphone input.
217	ATLAS_GPO2	O	2.7V	MC13783 general purpose output.
218	HP_OUTL	O	2.7V	Head Phone Out Left channel.
219	ATLAS_GPO1	O	2.7V	MC13783 general purpose output.
220	HP_OUTR	O	2.7V	Head Phone Out Right channel.
221	I2S/AC97_CLK (uP_SCK4)	I/O	2.7V_NVCC5,8	I2S Serial Clock signal.
222	CODEC_INL	I	2.7V	CODEC Left channel Line In.
223	I2S/AC97_FRAME (uP_SFS4)	O	2.7V_NVCC5,8	I2S Framing signal.
224	CODEC_INR	I	2.7V	CODEC Right channel Line In.
225	I2S/AC97_RX (uP_SRXD4)	I	2.7V_NVCC5,8	I2S data Receive signal.
226	CODEC_OUTL	O	2.7V	CODEC Left channel Line Out.
227	I2S/AC97_TX (uP_STXD4)	O	2.7V_NVCC5,8	I2S data Transmit signal.
228	CODEC_OUTR	O	2.7V	CODEC Right Channel Line Out.
229	DGND	I	GND	Ground. Connect to digital ground.
230	DGND	I	GND	Ground. Connect to digital ground.
231	RFU	I/O	NA	Reserved for future use. Do not connect.
232	RFU	I/O	NA	Reserved for future use. Do not connect.
233	RFU	I/O	NA	Reserved for future use. Do not connect.
234	RFU	I/O	NA	Reserved for future use. Do not connect.
235	RFU	I/O	NA	Reserved for future use. Do not connect.
236	RFU	I/O	NA	Reserved for future use. Do not connect.
237	RFU	I/O	NA	Reserved for future use. Do not connect.
238	RFU	I/O	NA	Reserved for future use. Do not connect.
239	RFU	I/O	NA	Reserved for future use. Do not connect.
240	RFU	I/O	NA	Reserved for future use. Do not connect.

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6 Mechanical Specifications

6.1 Interface Connectors

The i.MX31-10 SOM-LV connects to a PCB baseboard through two 240-pin board-to-board (BTB) socket connectors.

Ref Designator	Manufacturer	SOM-LV Connector P/N	Mating Connector P/N
J1, J2	Samtec	BTH-120-01-L-D-A	BSH-120-01-L-D-A

6.2 Mounting Specifications

6.2.1 Support Spacers

Attach spacers between the SOM-LV and application board to provide additional support when securing the SOM-LV to the baseboard.

Manufacturer	PN	Description	Sales Info.
Bivar	9908-5MM	Nylon screw (#4) spacers, 5 mm	http://www.bivar.com/distributors.asp

6.2.2 Screw Size

Securing the SOM-LV to the baseboard requires screws of size 3 or smaller.

6.2.3 Washers

Only use flat washers with diameters of 3.8 mm or smaller when securing the SOM-LV to the baseboard. Any other washer type or size may result in cut traces or component and PCB damage leaving the SOM-LV inoperable.

IMPORTANT NOTE: Do not apply an excessive amount of torque when securing the SOM-LV to the baseboard. Using more torque than necessary may damage the SOM-LV.

6.3 i.MX31 SOM-LV Mechanical Drawings

Please see the following two pages for mechanical drawings of the i.MX31 SOM-LV and recommended baseboard footprint layout.

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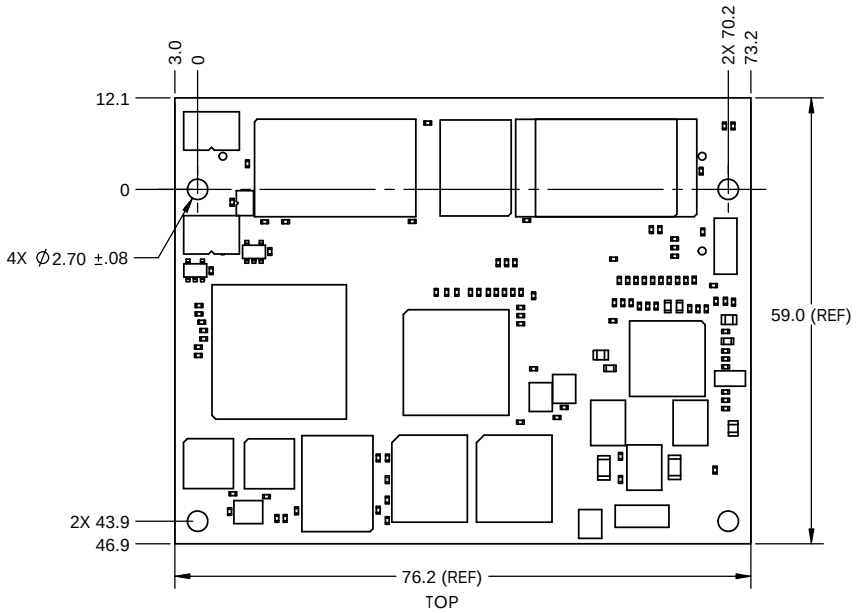
REVISIONS			
REV.	ECO NUMBER	DESCRIPTION	DATE
A	-	INITIAL RELEASE	07.30.08
B	-	UPDATED FOOTPRINT DIMENSIONING SCHEME	3.19.09



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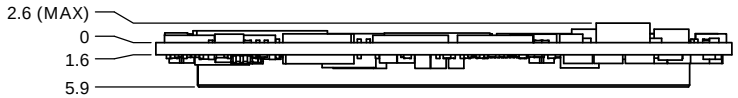

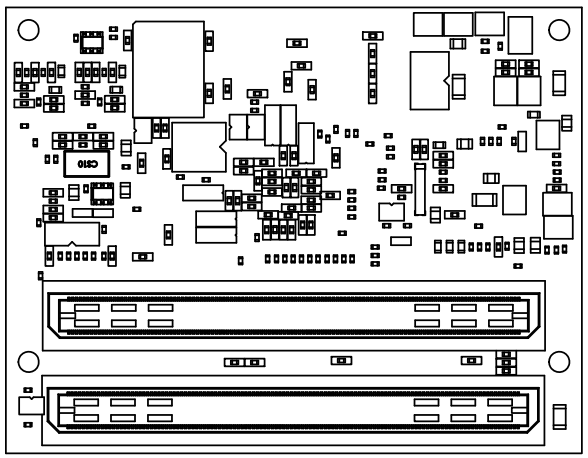

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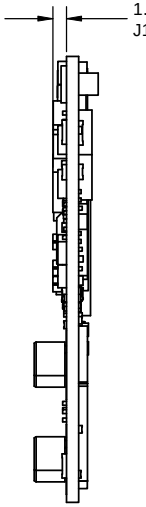


NOTES:

1. WITHIN LAYOUT AREA OF SOM-LV MAXIMUM COMPONENT HEIGHT ON APPLICATION BASEBOARD IS 1.0 MM
2. BASEBOARD CONNECTOR SPECIFICATION: SAMTEC BSH-120-01-L-D-A
3. DO NOT SCALE DRAWING

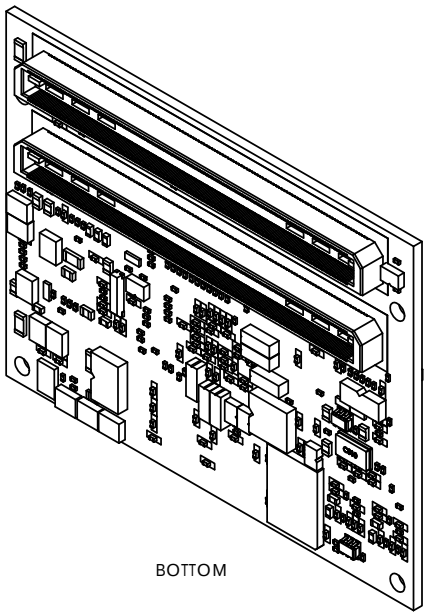
THIS DRAWING PREPARED IN ACCORDANCE WITH ASME Y14.5-2000

ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

TOLERANCES UNLESS OTHERWISE SPECIFIED
X ± 0.5
X.X ± 0.2
X.XX ± 0.1
X° ± 1°

THIRD ANGLE PROJECTION

ENG MHC	DATE 07.30.08	LOGIC 411 N. Washington Ave. Suite 400 Minneapolis, MN 55401 T: 612.672.9495 F: 612.672.9499 I: www.logicpd.com	SIZE C	TITLE i.MX31 SOM-LV	REV B
CHECK KAG	DATE 07.30.08				
MGR PMH	DATE 07.30.08		SCALE 2:1	DWG NO 1010496	SHEET 1 OF 2
MANF -	DATE -				



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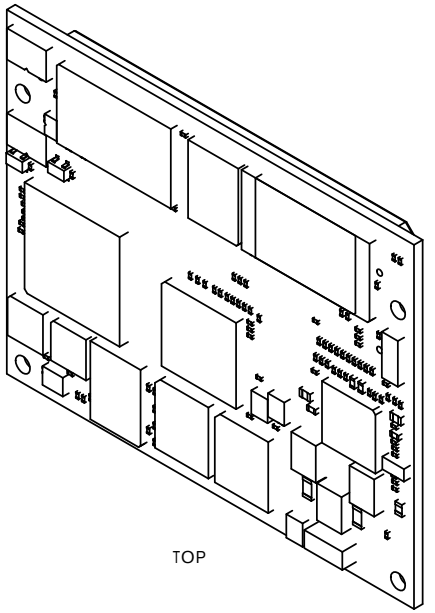

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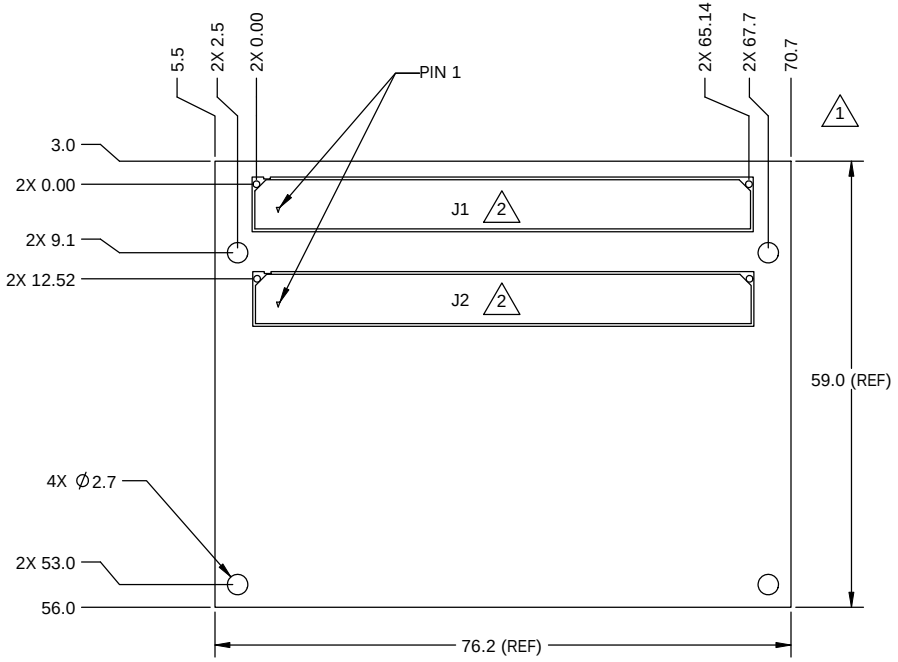
ISOMETRIC VIEWS
FOR REFERENCE ONLY



RECOMMENDED BASEBOARD FOOTPRINT

SIZE	TITLE	REV
C	i.MX31 SOM-LV	B
SCALE	DWG NO	SHEET
2:1	1010496	2 OF 2