KGF6N05D

N-Channel 5.5V Dual Power MOSFET

FN8788
Rev 1.00

The KGF6N05D is a dual 5.5V, 2.5mΩ, chip-scale, N-channel power MOSFET. The device uses technology that uniquely integrates low cost CMOS and LGA fabrication processes. The chip-scale WLCSP package offers small area, low vertical profile and is fully compatible with standard SMT assembly processes. The KGF6N05D device offers unprecedented low on-resistance and total gate charge, outperforming conventional trench MOSFETs and enabling high frequency, low voltage switching. The device offers extremely high power density, reducing the board size of DC/DC converters and other power management systems.

Features

- Industry leading figures of merit: $r_{DS(ON)} \times Q_g$ and $r_{DS(ON)} \times Q_{gd}$
- Low profile/small footprint chip-scale WLCSP package
- High frequency switching
- Known Good FET (KGF) Quality Assurance Process
- Low thermal resistance

Applications

- Point-of-load DC/DC converters
- Portable electronics
- OR'ing diodes

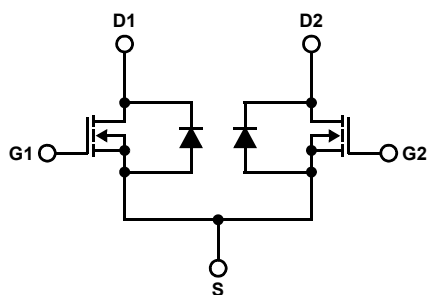| PRODUCT SUMMARY (PER FET)			
I_D	T_A = +25°C	6A	Maximum
$V_{(BR)DSS}$	I_D = 5mA	5.5V	Minimum
$r_{DS(ON)}$	V_{GS} = 4.5V	2.50mΩ	Typical
$r_{DS(ON)}$	V_{GS} = 4.5V (in Parallel)	1.25mΩ	Typical
Q_g	V_{GS} = 4.5V I_D = 6A	4.4nC	Typical
Q_{gd}		0.8nC	Typical

FIGURE 1. EQUIVALENT CIRCUIT

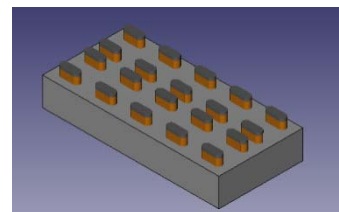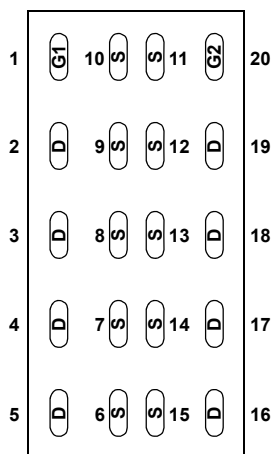FIGURE 2. WLCSP, DIE SIZE 2.475mm x 1.170mm

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)
KGF6N05D-400	T	-55°C to +150°C	20 Bump WLCSP

Pin Configuration

KGF6N05D
(20 BUMP WLCSP)
BOTTOM VIEW

Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	G1	Gate of MOSFET 1
2, 3, 4, 5	D1	Drain of MOSFET 1
6, 7, 8, 9, 10, 11, 12, 13, 14, 15	S	Source of both MOSFETs
16, 17, 18, 19	D2	Drain of MOSFET 2
20	G2	Gate of MOSFET 2

Absolute Maximum Ratings   (Note 1)

Drain-to-Source Voltage (V_{DS}) 5.5V
Gate-to-Source Voltage (V_{GS}) . . . . ±5.5V
Drain Current ($I_{D1} + I_{D2}$)
 Continuous (I_D) 12A
 Pulsed (I_{DM}) 40A
Single Pulse Avalanche Current (I_{AS}), ($I_{D1} + I_{D2}$)
 L ≤ 50µH, R_G ≤ 25Ω. 10A

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JP} (°C/W)
WLCSP Package	50	10

Maximum Power Dissipation (P_D) (Note 2)
 T_A = +25°C 2.5W (10s)
 T_A = +70°C 1.6W
Junction and Storage Temperature Range (T_J, T_{stg}). . . . .-55°C to +150°C
Pb-Free Reflow Profile . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. T_J = +25°C unless otherwise noted.
2. When mounted on 1 inch square 2oz copper clad FR-4.

Electrical Characteristics   Specifications are for single MOSFET unless otherwise specified. T_J = +25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 5mA	5.5			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 3.5V, V_{GS} = 0V, T_J = +25°C			1	µA
		V_{DS} = 5.5V, V_{GS} = 0V, T_J = +25°C			12	
		V_{DS} = 5.5V, V_{GS} = 0V, T_J = +125°C			125	
I_{GSS}	Gate-Body Leakage	V_{GS} = 5.5V, V_{DS} = 0V			75	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.60	0.75	0.90	V
$r_{DS(ON)}$	Drain-to-Source On-State Resistance (per MOSFET)	V_{GS} = 3.5V, I_D = 6A		2.7	3.4	mΩ
		V_{GS} = 4.5V, I_D = 6A		2.5	3.0	mΩ
$r_{DS(ON)}$	Drain-to-Source On-State Resistance (in Parallel)	V_{GS} = 3.5V, I_D = 6A		1.35	1.7	mΩ
		V_{GS} = 4.5V, I_D = 6A		1.25	1.5	mΩ
C_{iss}	Input Capacitance	V_{DS} = 5.5V, V_{GS} = 0V, f = 1MHz		552	630	pF
C_{oss}	Output Capacitance			689	787	pF
C_{rss}	Reverse Transfer Capacitance			175	201	pF
C_{iss}	Input Capacitance	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz		606	663	pF
C_{oss}	Output Capacitance			970	1206	pF
C_{rss}	Reverse Transfer Capacitance			218	268	pF
R_g	Gate Resistance	V_{DS} = 0V, f = 1MHz		0.6		Ω
Q_g	Total Gate Charge	V_{GS} = 3.5V, I_D = 6A, V_{DS} = 4.4V		3.5	4.0	nC
Q_{gs}	Gate-to-Source Charge			0.5	1.0	nC
Q_{gd}	Gate-to-Drain Charge			0.8	1.3	nC
Q_g	Total Gate Charge	V_{GS} = 4.5V, I_D = 6A, V_{DS} = 4.4V		4.4	4.7	
t_{rr}	Source-to-Drain Reverse Recovery Time	I_S = 3A, di/dt = 33A/µs		59		ns
V_{SD}	Diode Forward Voltage	I_S = 3A, V_{GS} = 0V		0.69	1.00	V

NOTE:

3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

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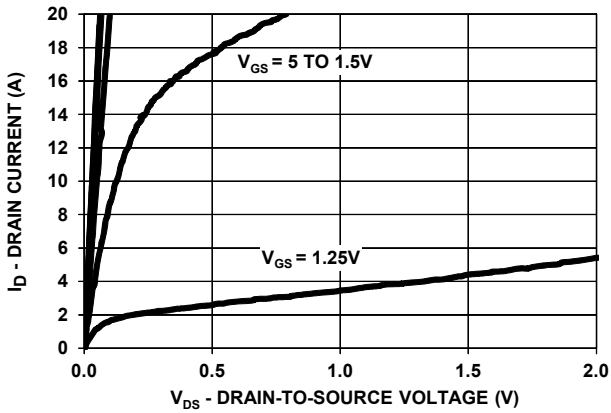# Typical Performance Curves

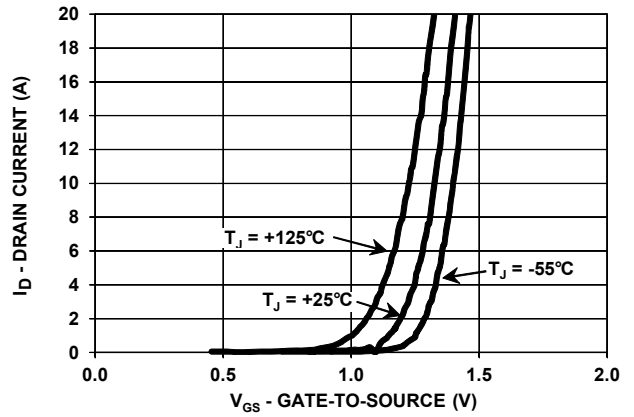
FIGURE 3. OUTPUT CHARACTERISTICS
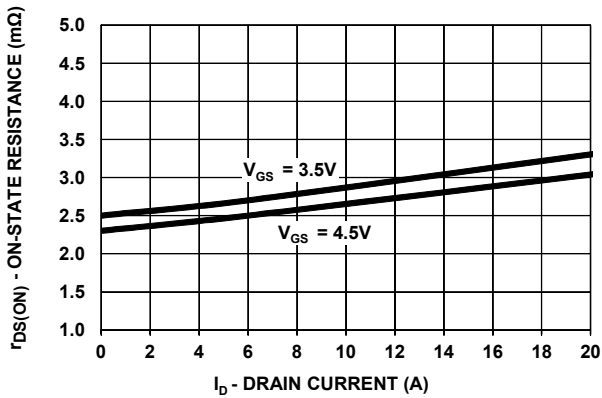

FIGURE 4. TRANSFER CHARACTERISTICS

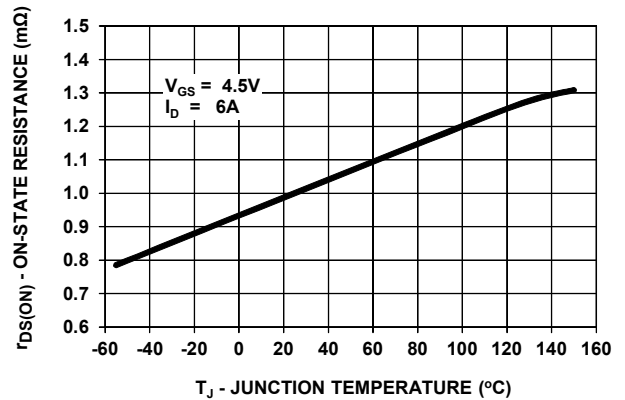FIGURE 5. DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

FIGURE 6. DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE
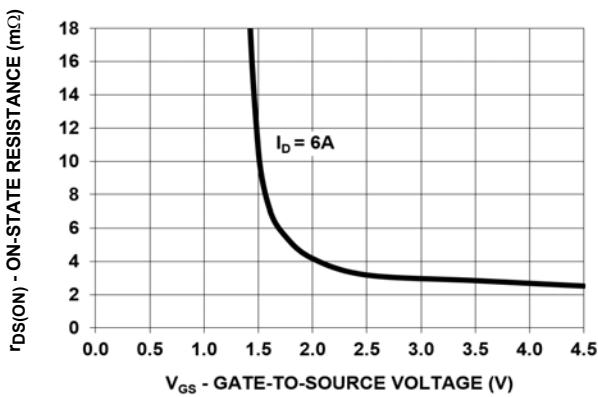

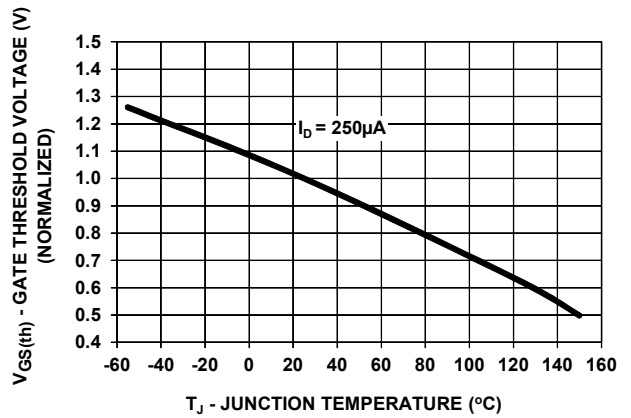FIGURE 7. DRAIN-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

FIGURE 8. GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE
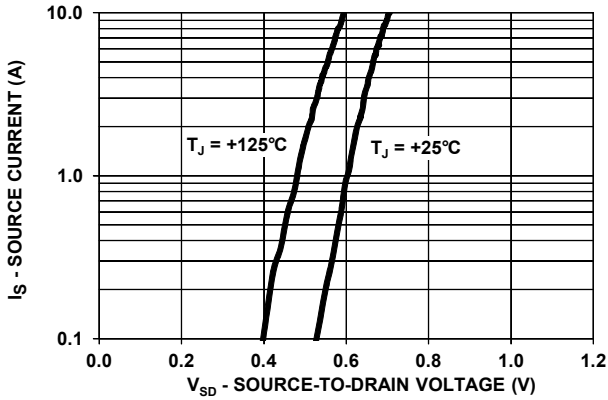
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Typical Performance Curves (Continued)
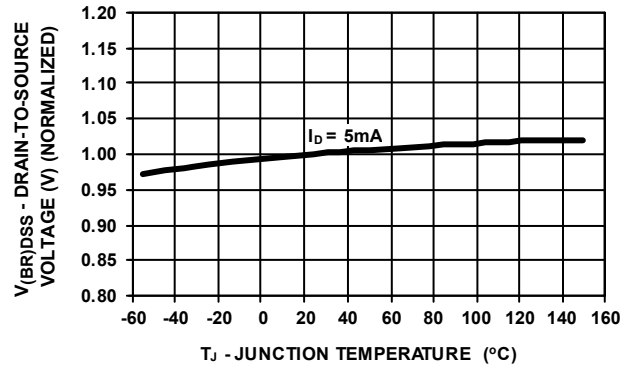

FIGURE 9. SOURCE-TO-DRAIN DIODE FORWARD VOLTAGE

FIGURE 10. DRAIN-TO-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE
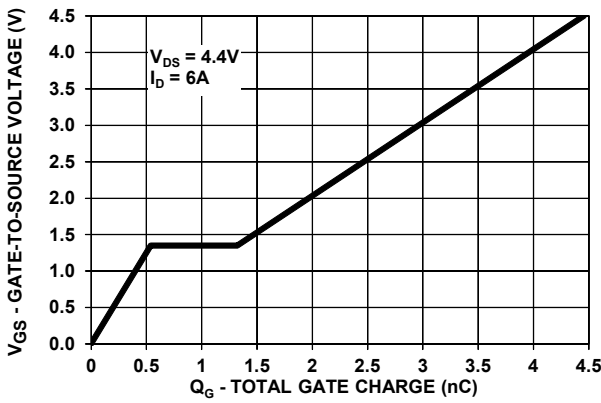
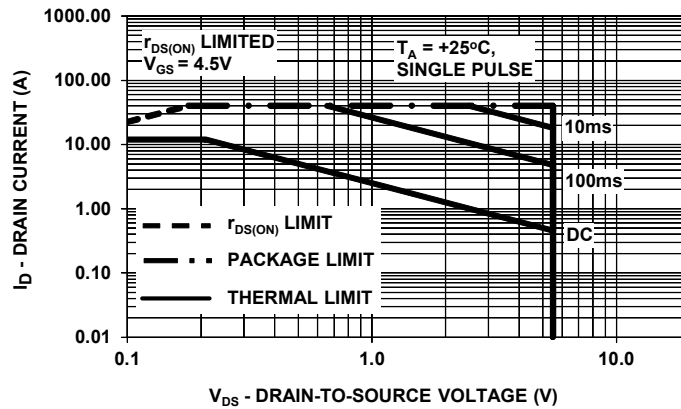FIGURE 11. GATE CHARGE
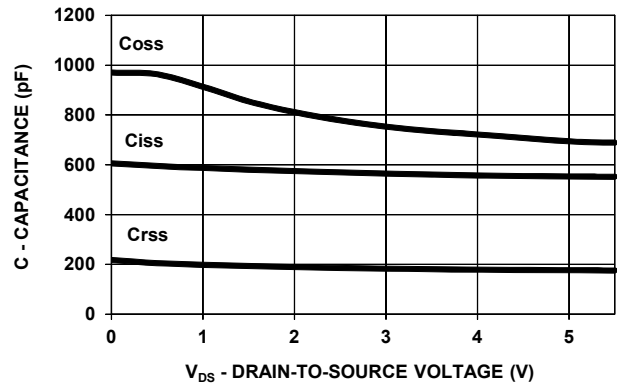
FIGURE 12. CAPACITANCE

FIGURE 13. MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA (IN PARALLEL)

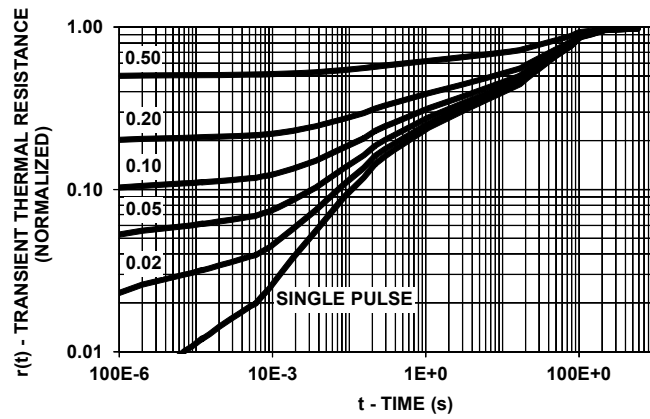# Typical Performance Curves (Continued)

FIGURE 14. TRANSIENT THERMAL RESPONSE, JUNCTION-TO-AMBIENT (IN PARALLEL)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 18, 2015	FN8788.1	Added "Note 1. T_J = +25°C unless otherwise noted." to Abs Max on page 3.
October 30, 2015	FN8788.0	Initial release

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Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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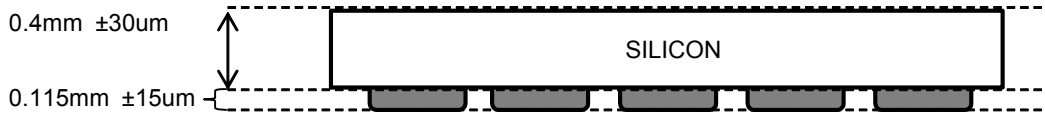For additional products, see www.intersil.com/en/products.html

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Dimensional Outline and Pad Layout

Side View

0.4mm ±30um

SILICON

0.115mm ±15um

Pad-up View

0.5mm

D D D D G1

0.1mm

0.335mm

1.170mm ±15um

0.2mm

S S S S S

S S S S S

D D D D G2

0.27mm

2.475mm ±15um

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