# Stratix III 3SL150 Development Board

## Reference Manual

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# Contents

## Additional Information

# 1. Overview

## Introduction

This document describes the hardware features of the Stratix® III development board, including detailed pin-out information to enable you to create custom FPGA designs that interface with all components of the board.

For information about setting the Stratix III development board and using the kit's demo software, refer to the *Stratix III Development Kit User Guide*.

## General Description

The Stratix III development board provides a hardware platform for developing and prototyping low-power, high-performance, and logic-intensive designs. The board provides a wide range of peripherals and memory interfaces to facilitate the design and development of Stratix III FPGA designs. Additionally, two high-speed mezzanine card (HSMC) connectors are available to add additional functionality via a variety of HSMCs available from both Altera and various partners.

To see a list of the latest available HSMC cards and to request a copy of the HSMC specification, visit www.altera.com.

Design advancements and innovations, such as Programmable Power Technology and selectable core voltage, ensure that designs implemented in Stratix III FPGAs operate faster, but consume less power than previous generation Stratix devices.

For more information about Stratix III device Programmable Power Technology, refer to the following documents:

- Stratix III Programmable Power White Paper
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*

With up to 7,280 KByte of enhanced TriMatrix memory and 384 embedded 18 × 18 multipliers, the on-board Stratix III device supplies internal memory while also providing I/O support for a variety of SDRAM (DDR2 or DDR3) and SRAM (QDRII or RLDRAM II) interfaces. Both DDR2 and QDRII are available on the Stratix III development board providing a high bandwidth, high-speed and low-latency solution.

The Stratix III development board is especially suitable for high-performance, logic-rich applications that require stringent signal and power integrity solutions. For example, the wireless, broadcast, and military markets require advanced signal processing techniques and very low power consumption, while also demanding flexibility and adaptability in the field.

For more information about:

- External memory interfaces in Stratix III devices, refer to the *External Memory Interfaces* chapter in the *Stratix III Device Handbook*
- The Altera DDR and DDR2 SDRAM Controller Compiler MegaCore© function, refer to the *DDR and DDR2 SDRAM Controller Compiler User Guide*
- Power optimization, refer to *AN 437: Power Optimization Techniques in Stratix III FPGAs*
- Altera Video and Image Processing Suite MegaCore functions, refer to the *Video and Image Processing Suite User Guide*

## Board Component Blocks

The board features the following major component blocks:

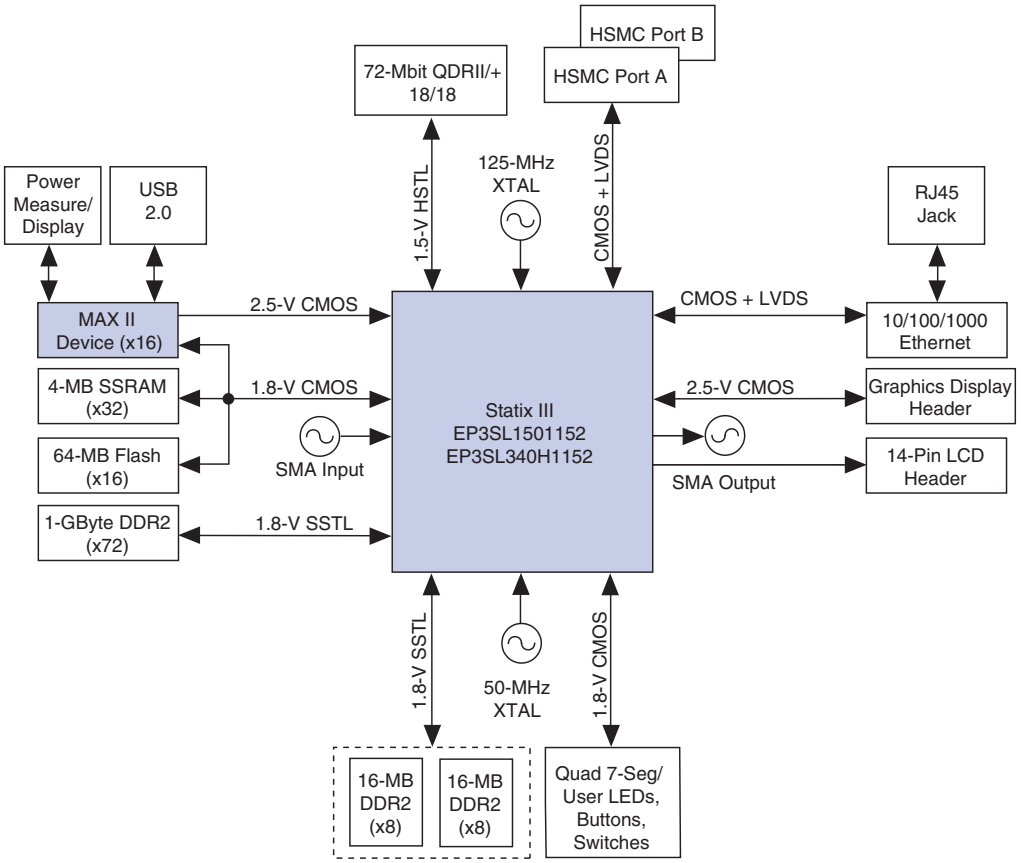
- 1,152-pin Altera Stratix III EP3SL150F FPGA in a ball-grid array (BGA) package
  - 142,000 logic elements (LEs)
  - 5,499 Kbits of memory
  - 384 multiplier blocks
  - Eight phase locked loops (PLLs)
  - 16 global clock networks
  - 736 user I/Os
  - 1.1-V core power
- 256-pin Altera EPM2210GF256 CPLD in a BGA package
  - 1.8-V core power
- On-board memory
  - 1-GByte DDR2 SDRAM DIMM
  - 72-Mbit QDRII/+ SRAM
  - 16-MByte DDR2 SDRAM devices
    - Individually addressable
  - 4-MByte SSRAM
  - 64-MByte flash memory
- FPGA configuration circuitry
  - MAX® II CPLD and flash passive serial configuration
  - On-board USB-Blaster™ circuitry using the Quartus II Programmer

- On-board clocking circuitry
  - Two clock oscillators to support Stratix III device user logic
    - 125 MHz
    - 50 MHz
  - SMA connector for external clock input and output
- General user and configuration interfaces
  - LEDs/displays:
    - Eight user LEDs
    - One configuration-done LED
    - One transmit/receive LED (TX/RX) per HSMC interface
    - One HSMC-present LED per HSMC interface
    - Six Ethernet LEDs
    - User Quad 7-segment display
    - Power consumption display
  - Push-buttons:
    - User reset push-button (CPU reset)
    - Four general user push-buttons
    - System reset push-button (user configuration)
    - One factory push-button switch (factory configuration)
  - DIP switches:
    - MAX II control DIP switch
    - Eight user DIP switches
  - Speaker header
- Displays
  - 128 × 64 graphics LCD
  - 16 × 2 line character LCD
- Power supply
  - 14-V – 20-V DC input
  - On-board power measurement circuitry
  - Up to 20 W per HSMC interface
- Mechanical
  - 7 in. × 8.25 in. board
  - Bench-top design

## Block Diagram

Figure 1–1 shows the functional block diagram of the Stratix III development board.

**Figure 1–1. Stratix III Development Board Block Diagram**




# Handling the Board

When handling the board, it is important to observe the following precaution:

CAUTION

Static Discharge Precaution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

# 2. Board Components

## Introduction

This chapter introduces the important components on the Stratix III development board. Figure 2–1 illustrates component locations and Table 2–1 describes component features.

This chapter consists of the following sections:



A complete set of board schematics, a physical layout database, and GERBER files for the Stratix III development board reside in the Stratix III Development Kit documents directory.

For information about powering up the development board and installing the demo software, refer to the *Stratix III Development Kit User Guide*.

## Board Overview

This section provides an overview of the Stratix III development board, including an annotated board image and component descriptions.

Figure 2–1 shows the top view of the Stratix III development board.

**Figure 2–1. Top View of the Stratix III Development Board**

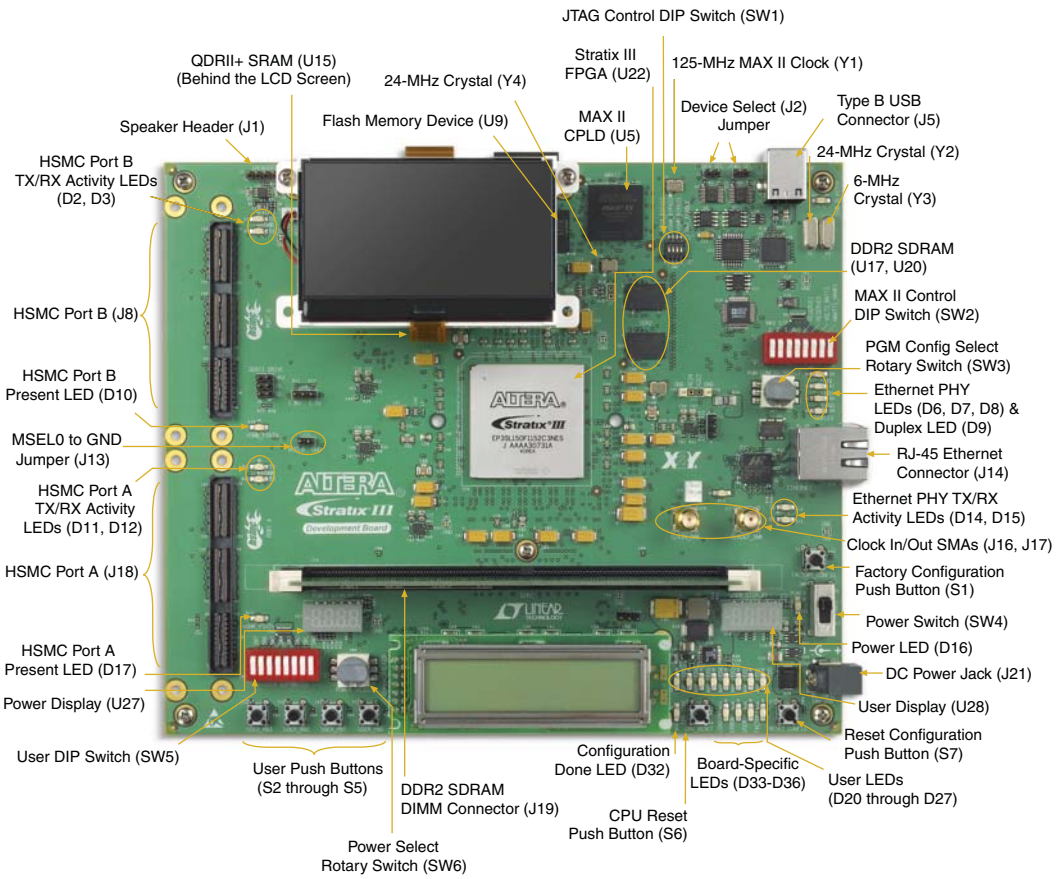



Table 2–1 describes the components and lists their corresponding board references.

**Table 2–1. Stratix III Development Board (Part 1 of 3)**

| Board Reference | Type | Description |
|---|---|---|
| **Featured Devices** | | |
| U22 | FPGA | EP3SL150F1152, 1152-pin BGA package. |
| U5 | CPLD | EPM2210GF256, 256-pin device in a BGA package. |
| **Configuration Status and Setup Elements** | | |
| J2 | Device select (DEV_SEL) jumper | Sets target device for JTAG signals when using an external USB Blaster or equivalent. |
| J5 | Input | Type B USB connector that allows for connecting a Type A-B USB cable between a PC and the board. |
| D32 | Configuration done LED | Green LED that illuminates when the FPGA is successfully configured. |
| D11, D12 (Port A)<br>D2, D3 (Port B) | Channel activity LEDs | Green LEDs that indicate the RX and TX activity on the HSMC Ports A or B. |
| J1 | Header | Speaker header. |

**Table 2–1. Stratix III Development Board (Part 2 of 3)**

| Board Reference | Type | Description |
|---|---|---|
| D6, D7, D8 | Ethernet PHY LEDs | Green Ethernet PHY LEDs. Illuminate when Ethernet PHY is using the 10/100/1000 Mbps (D6, D7, D8) connection speeds. |
| D9 | Duplex Ethernet PHY LED | Green Ethernet PHY LED. Illuminates when Ethernet PHY is both sending and receiving data. |
| D16 | Power LED | Blue LED indicates when power is applied to the board. |
| D14, D15 | Ethernet PHY transmit/receive activity LEDs | Green LEDs. Illuminates when transmit/receive data is active from the Ethernet PHY. |
| SW2 | MAX II Control DIP switch | Controls various features of the MAX II device specific to the Stratix III development board. |
| SW1 | JTAG control DIP switch | JTAG control DIP switch used to remove or include devices in the active JTAG chain. |
| U27 | Power display | Displays power measured by the MAX II CPLD. |
| D11, D12 | HSMC Port A transmit/receive activity LEDs | Illuminates when transmit/receive data is active from the HSMC Port A. |
| D2, D3 | HSMC Port B transmit/receive activity LEDs | Illuminates when transmit/receive data is active from the HSMC Port B. |
| **Clock Circuitry** | | |
| Y1 | 125 MHz | MAX II 125-MHz device clock. |
| Y2 | 24-MHz crystal | Cypress USB PHY. |
| Y3 | 6-MHz crystal | USB PHY FTDI reference clock. |
| Y4 | 24 MHz | MAX II 24-MHz device clock. |
| Y5 | 125 MHz | 125-MHz clock oscillator used for the system clock. |
| Y6 | 50 MHz | 50-MHz clock oscillator used for data processing. |
| J16 | SMA clock input | SMA connector that allows the provision of an external clock input. |
| J17 | SMA clock output | SMA connector that allows the provision of an external clock output. |
| **General User Input and Output** | | |
| S2 through S5 | User push-buttons | Four 2.5-V push-button switches for user-defined, logic inputs. |
| S6 | CPU reset push-button | One 2.5-V push-button switch for FPGA logic and CPU reset. |
| S1 and S7 | Reset and factory configuration push-button | Two 2.5-V push-button switches that control FPGA configuration from flash memory. |
| D20 through D27 | User LEDs | Eight user-defined LEDs. |
| SW3 | PGM Config Select rotary switch | Rotary switch to select which FPGA configuration file is loaded from the flash device into the FPGA. |
| SW6 | Power Select rotary switch | Power rail select for on-board power monitor. |
| U28 | User display | User-defined, green 7-segment display. |
| SW5 | User DIP switch | User-defined, eight position DIP switch. |
| **Memory** | | |
| U9 | Flash | 512 Mbits of flash memory. |
| U4, U10 | P-SRAM | The P-SRAM devices connect to the MAX II device as well as the flash memory device. |
| U17, U20 | DDR2 SDRAM | Two 16M × 8, 1.8-V core devices in 60-pin FBGA packages. |

**Table 2–1. Stratix III Development Board (Part 3 of 3)**

| Board Reference | Type | Description |
|---|---|---|
| U15 | QDRII | Burst-of-four, 2M × 18, 400-MHz QDRII memory interface in an FBGA package. |
| J19 | DDR2 SDRAM DIMM | Connector for 1 GByte × 72 DDR2 SDRAM DIMM. |
| **Components and Interfaces** | | |
| U11 | USB device | USB device that provides JTAG programming of on-board devices, including the Stratix III device and flash memory device. |
| J14 | Ethernet cable jack | The RJ-45 jack is for Ethernet cable connection. The connector is fed by a 10/100/1000 base T PHY device with an RGMII interface to the Stratix III device. |
| J8 and J18 | HSMC Port A and Port B | HSMC connectors to allow for expansion via the addition of HSMCs. |
| **Power Supply** | | |
| J21 | DC power jack | 14–20 V DC power source. |
| SW4 | Input | Switches the board's power on and off. |

# Featured FPGA (U22)

The Stratix III Development Kit features the EP3SL150F1152C2 device (U22) in a 1152-pin BGA package.

For more information about Stratix III devices, refer to the *Stratix III Device Handbook*.

Table 2–2 lists the main Stratix III EP3SL150 device features.

**Table 2–2. Stratix III EP3SL150 Device Features**

| ALMs | LEs | M9K Blocks | M144K Blocks | MLAB Blocks | Total Embedded RAM Kbits | MLAB Kbits | Total Memory Kbits | 18 × 18 Bit Multipliers | PLLs |
|---|---|---|---|---|---|---|---|---|---|
| 57 | 142.5 | 355 | 16 | 2,850 | 5,499 | 1,781 | 7,280 | 384 | 8 |

Table 2–3 lists the Stratix III device component reference and manufacturing information.

**Table 2–3. Stratix III Device Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U22 | High-speed, low-power FPGA | Altera Corporation | EP3SL150F1152 | www.altera.com |

Table 2–4 lists the Stratix III device EP3SL150F1152 pin count.

**Table 2–4. Stratix III Device Pin Count (Part 1 of 2)**

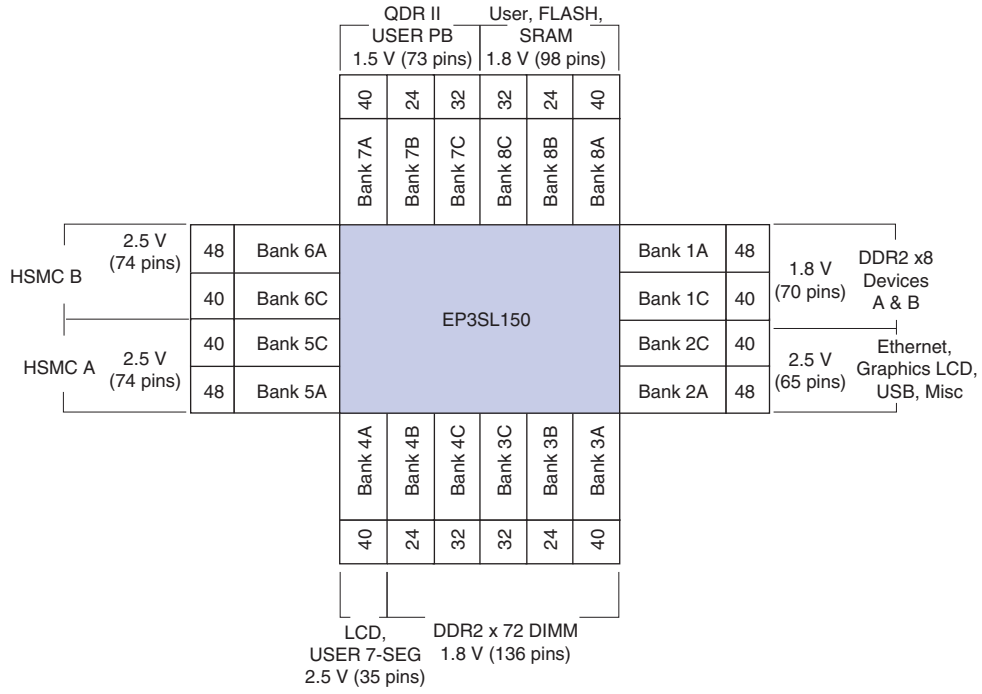
| Function | I/O Type | I/O Count | Special Pins |
|---|---|---|---|
| Oscillators and SMAs | 1.8-V CMOS | 4 | Three clock inputs, one output |
| DDR2 DIMM | 1.8-V SSTL | 136 | 18 data strobe signal (DQS) pins |
| DDR2 devices | 1.8-V SSTL | 74 | Four DQS pins |

**Table 2–4. Stratix III Device Pin Count (Part 2 of 2)**

| Function | I/O Type | I/O Count | Special Pins |
|---|---|---|---|
| QDRII+ | 1.5-V/1.8-V HSTL | 66 | Two CQ pins |
| Flash/P-SRAM/MAX | 1.8-V CMOS | 79 | — |
| Ethernet | 2.5-V CMOS<br>2.5-V LVDS | 36 | 6, 2.5 V LVDS |
| User I/O (LEDs, etc) | 1.8-V/2.5 V | 30 | — |
| 14-pin LCD header | 2.5-V CMOS | 11 | — |
| Graphics display | 2.5-V CMOS | 16 | — |
| USB | 2.5-V CMOS | 0 | — |
| HSMC Port A | 2.5-V CMOS<br>2.5-V LVDS | 88 | 3 clock inputs |
| HSMC Port B | 2.5-V CMOS<br>2.5-V LVDS | 88 | 3 clock inputs |
| Device I/O total: 628<br>Stratix III device I/O total: 736 | | | |

Figure 2–2 shows the EP3SL150 I/O bank diagram from a system perspective.

**Figure 2–2. System I/O Bank Diagram**




For additional information about Altera devices, go to www.altera.com/products/devices.

## Device Support

Although the target FPGA for the Stratix III development board is the EP3SL150 device, which is the first device in the 65 nm Stratix III FPGA device family, the board is also designed to migrate to the Stratix III EP3SL340H1152 device.

The following list shows the main power rails for the target device:

- 0.9-V/1.1-V $V_{CCL}$
- 1.1-V $V_{CC}$
- 2.5-V $V_{CCPT}$
- 1.8-V/2.5-V/3.0-V $V_{CCPGM}$
- 2.5-V/3.0-V $V_{CCPD}$
- 2.5-V $V_{CCA\_PLL}$
- 2.5-V $V_{CC\_CLKIN}$
- 2.5-V $V_{CCBAT}$
- 1.2-V to 3.3-V $V_{CCIO}$

The board's target device, the EP3SL150F1152C2, comprises the following:

- 57,000 adaptive logic modules (ALMs)
- 142,000 LEs
- 1,775 KBytes of RAM
- 736 user I/O
- 8 PLLs
- 16 global clocks
- 384 18 × 18 multipliers in finite impulse response (FIR) mode

The board is designed to migrate to the EP3SL340H1152C3 device, which provides the following features in the H1152 package:

- 135,000 ALMs
- 338,000 LEs
- 4,225 KBytes of RAM
- 736 user I/O
- 8 PLLs
- 16 global clocks
- 576 18 × 18 multipliers in FIR mode

## I/O Resources

This section lists specific I/O resources available with the EP3SL150F1152 device, which is from the L family of Stratix III devices.

Table 2–3 shows the configuration of the 20 user I/O banks and each bank's I/O count for the EP3SL150 device. Incidentally, within the same package, the EP3SL150 and the EP3SL340 devices have the same number of PLLs, user I/O banks, and user I/Os.

**Figure 2–3. EP3SL150F1152 Device I/O Bank Resources**

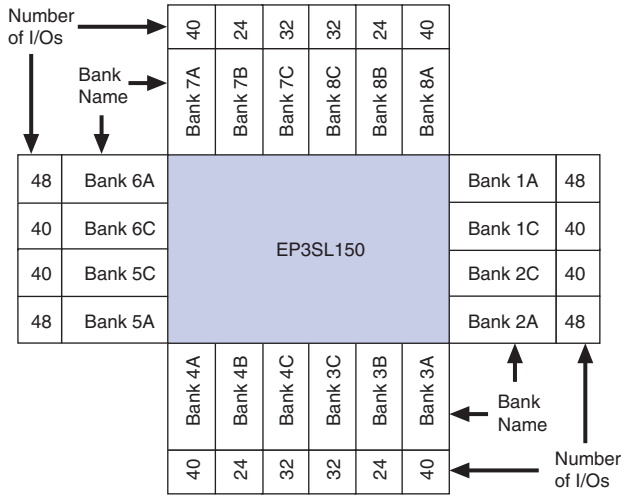
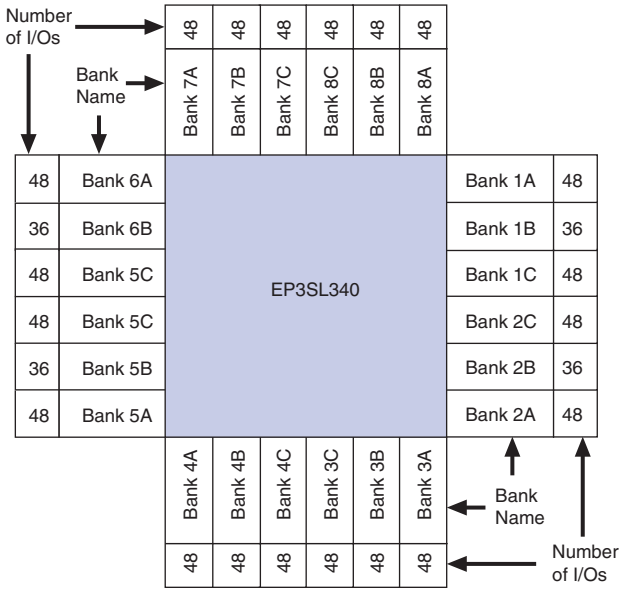



Figure 2–4 shows the configuration of the 24 possible user I/O banks and each bank's I/O count for the EP3SL340 device in its largest package. Banks 1B, 2B, 5B, and 6B are not available in the F1152 package.

**Figure 2–4. EP3SL340F1517 Device I/O Bank Diagram**



# MAX II CPLD

The board utilizes an Altera MAX II CPLD (U5) for the following purposes:

- Power-up configuration of the FPGA from flash memory
- Embedded USB-Blaster core for USB-based configuration of the FPGA
- Power consumption monitoring and display

Additionally, the MAX II device is also used to help dual-footprint the FTDI USB device and Cypress USB device. Each device has a shared path between the USB device and the MAX II CPLD. This path then drives to the FPGA separately. Figure 2–5 illustrates the MAX II device's functional block diagram.

**Figure 2–5. MAX II Device's Block Diagram**

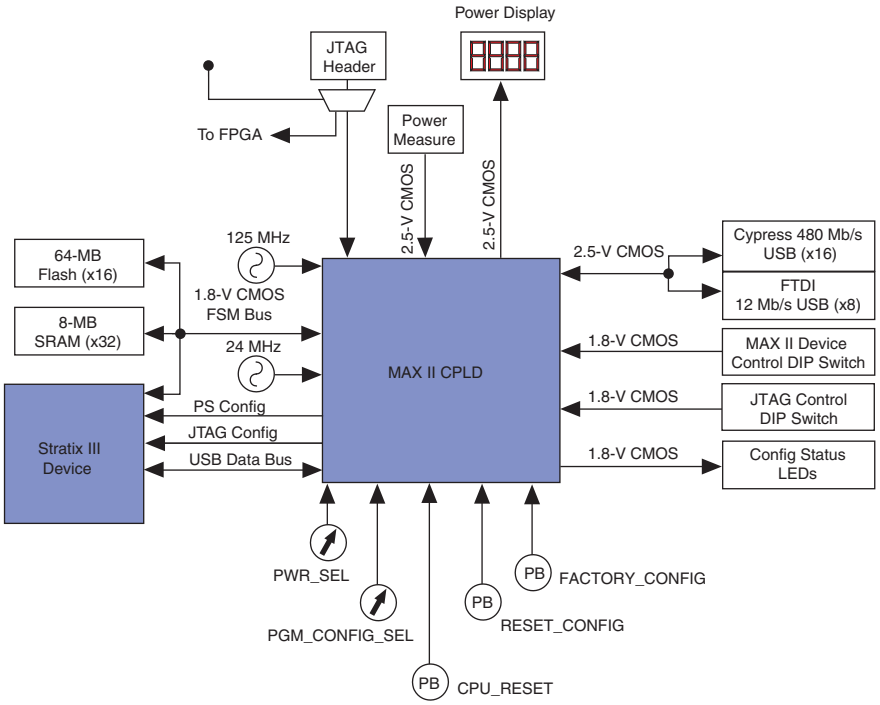



Table 2–5 lists the I/O signals present on the MAX II CPLD. The signal names and functions are relative to the MAX II device (U5).

**Table 2–5. MAX II Device Pin-out (Part 1 of 9)**

| MAX II Pin Number | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| N9 | Address bus shared with flash and P-SRAM bit 0 | FSM_A0 | 1.8 V | F22 | U9 pin A1 |
| T8 | Address bus shared with flash and P-SRAM bit 1 | FSM_A1 | 1.8 V | H23 | U9 pin B1 and U4 pin A3 and U10 pin A3 |
| T9 | Address bus shared with flash and P-SRAM bit 2 | FSM_A2 | 1.8 V | G23 | U9 pin C1 and U4 pin A4 and U10 pin A4 |

**Table 2–5. MAX II Device Pin-out (Part 2 of 9)**

| MAX II Pin Number | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| R9 | Address bus shared with flash and P-SRAM bit 3 | FSM_A3 | 1.8 V | F23 | U9 pin D1 and U4 pin A5 and U10 pin A5 |
| P9 | Address bus shared with flash and P-SRAM bit 4 | FSM_A4 | 1.8 V | D27 | U9 pin D2 and U4 pin B3 and U10 pin B3 |
| T10 | Address bus shared with flash and P-SRAM bit 5 | FSM_A5 | 1.8 V | D28 | U9 pin A2 and U4 pin B4 and U10 pin B4 |
| P13 | Address bus shared with flash and P-SRAM bit 6 | FSM_A6 | 1.8 V | F25 | U9 pin C2 and U4 pin C3 and U10 pin C3 |
| R10 | Address bus shared with flash and P-SRAM bit 7 | FSM_A7 | 1.8 V | F26 | U9 pin A3 and U4 pin C4 and U10 pin C4 |
| M10 | Address bus shared with flash and P-SRAM bit 8 | FSM_A8 | 1.8 V | G24 | U9 pin B3 and U4 pin D4 and U10 pin D4 |
| T11 | Address bus shared with flash and P-SRAM bit 9 | FSM_A9 | 1.8 V | F24 | U9 pin C3 and U4 pin H2 and U10 pin H2 |
| N10 | Address bus shared with flash and P-SRAM bit 10 | FSM_A10 | 1.8 V | E26 | U9 pin C4 and U4 pin H3 and U10 pin H3 |
| R11 | Address bus shared with flash and P-SRAM bit 11 | FSM_A11 | 1.8 V | D26 | U9 pin C4 and U4 pin H4 and U10 pin H4 |
| P10 | Address bus shared with flash and P-SRAM bit 12 | FSM_A12 | 1.8 V | A30 | U9 pi A12 and U4 pin H5 and U10 pin H5 |
| T12 | Address bus shared with flash and P-SRAM bit 13 | FSM_A13 | 1.8 V | A33 | U9 pin B5 and U4 pin G3 and U10 pin G3 |
| M11 | Address bus shared with flash and P-SRAM bit 14 | FSM_A14 | 1.8 V | B31 | U9 pin C5 and U4 pin G4 and U10 pin G4 |
| R12 | Address bus shared with flash and P-SRAM bit 15 | FSM_A15 | 1.8 V | A31 | U9 pin D7 and U4 pin F3 and U10 pin F3 |
| N11 | Address bus shared with flash and P-SRAM bit 16 | FSM_A16 | 1.8 V | B32 | U9 pin D8 and U4 pin F4 and U10 pin F4 |
| T13 | Address bus shared with flash and P-SRAM bit 17 | FSM_A17 | 1.8 V | A32 | U9 pin A7 and U4 pin E4 and U10 pin E4 |
| P11 | Address bus shared with flash and P-SRAM bit 18 | FSM_A18 | 1.8 V | M23 | U9 pin B7 and U4 pin D3 and U10 pin D3 |
| R13 | Address bus shared with flash and P-SRAM bit 19. | FSM_A19 | 1.8 V | L23 | U9 pin C7 and U4 pin H1 and U10 pin H1 |
| M12 | Address bus shared with flash and P-SRAM bit 20 | FSM_A20 | 1.8 V | B29 | U9 pin C8 and U4 pin G2 and U10 pin G2 |
| R14 | Address bus shared with flash and P-SRAM bit 21 | FSM_A21 | 1.8 V | C29 | U9 pin A8 and U4 pin H6 and U10 pin H6 |
| N12 | Address bus shared with flash and P-SRAM bit 22 | FSM_A22 | 1.8 V | C31 | U9 pin G1 |

**Table 2–5. MAX II Device Pin-out (Part 3 of 9)**

| MAX II Pin Number | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| T15 | Address bus shared with flash and P-SRAM bit 23 | FSM_A23 | 1.8 V | D31 | U9 pin H8 |
| P12 | Address bus shared with flash and P-SRAM bit 24 | FSM_A24 | 1.8 V | F27 | U9 pin B6 |
| P4 | Data bus shared with flash and SRAM bit 0 | FSM_D0 | 1.8 V | G27 | U9 pin F2 and U4 pin B6 |
| R1 | Data bus shared with flash and SRAM bit 1 | FSM_D1 | 1.8 V | F28 | U9 pin E2 and U4 pin C5 |
| P5 | Data bus shared with flash and SRAM bit 2 | FSM_D2 | 1.8 V | E28 | U9 pin G3 and U4 pin C6 |
| T2 | Data bus shared with flash and SRAM bit 3 | FSM_D3 | 1.8 V | D30 | U9 pin E4 and U4 pin D5 |
| N5 | Data bus shared with flash and SRAM bit 4 | FSM_D4 | 1.8 V | C30 | U9 pin E5 and U4 pin E5 |
| R3 | Data bus shared with flash and SRAM bit 5 | FSM_D5 | 1.8 V | F29 | U9 pin G5 and U4 pin F5 |
| P6 | Data bus shared with flash and SRAM bit 6 | FSM_D6 | 1.8 V | E29 | U9 pin G6 and U4 pin F6 |
| R4 | Data bus shared with flash and SRAM bit 7 | FSM_D7 | 1.8 V | J24 | U9 pin H7 and U4 pin G6 |
| N6 | Data bus shared with flash and SRAM bit 8 | FSM_D8 | 1.8 V | J25 | U9 pin E1 and U4 pin B1 |
| T4 | Data bus shared with flash and SRAM bit 9 | FSM_D9 | 1.8 V | A24 | U9 pin E3 and U4 pin C1 |
| M6 | Data bus shared with flash and SRAM bit 10 | FSM_D10 | 1.8 V | A26 | U9 pin F3 and U4 pin C2 |
| R5 | Data bus shared with flash and SRAM bit 11 | FSM_D11 | 1.8 V | B25 | U9 pin F4 and U4 pin D2 |
| P7 | Data bus shared with flash and SRAM bit 12 | FSM_D12 | 1.8 V | A25 | U9 pin F5 and U4 pin E2 |
| T5 | Data bus shared with flash and SRAM bit 13 | FSM_D13 | 1.8 V | J20 | U9 pin H5 and U4 pin F2 |
| N7 | Data bus shared with flash and SRAM bit 14 | FSM_D14 | 1.8 V | K20 | U9 pin G7 and U4 pin F1 |
| R6 | Data bus shared with flash and SRAM bit 15 | FSM_D15 | 1.8 V | K21 | U9 pin E7 and U4 pin G1 |
| M7 | Data bus shared with flash and SRAM bit 16 | FSM_D16 | 1.8 V | K22 | U10 pin B6 |
| T6 | Data bus shared with flash and SRAM bit 17 | FSM_D17 | 1.8 V | C26 | U10 pin C5 |
| P14 | Data bus shared with flash and SRAM bit 18 | FSM_D18 | 1.8 V | B26 | U10 pin C6 |
| R7 | Data bus shared with flash and SRAM bit 19 | FSM_D19 | 1.8 V | J22 | U10 pin D5 |

**Table 2–5. MAX II Device Pin-out (Part 4 of 9)**

| MAX II Pin Number | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| P8 | Data bus shared with flash and SRAM bit 20 | FSM_D20 | 1.8 V | J21 | U10 pin E5 |
| T7 | Data bus shared with flash and SRAM bit 21 | FSM_D21 | 1.8 V | C24 | U10 pin F5 |
| N8 | Data bus shared with flash and SRAM bit 22 | FSM_D22 | 1.8 V | E25 | U10 pin F6 |
| R8 | Data bus shared with flash and SRAM bit 23 | FSM_D23 | 1.8 V | D25 | U10 pin G6 |
| F12 | Data bus shared with flash and SRAM bit 24 | FSM_D24 | 1.8 V | D24 | U10 pin B1 |
| D16 | Data bus shared with flash and SRAM bit 25 | FSM_D25 | 1.8 V | A27 | U10 pin C1 |
| F13 | Data bus shared with flash and SRAM bit 26 | FSM_D26 | 1.8 V | A29 | U10 pin C2 |
| D15 | Data bus shared with flash and SRAM bit 27 | FSM_D27 | 1.8 V | C27 | U10 pin D2 |
| F14 | Data bus shared with flash and SRAM bit 28 | FSM_D28 | 1.8 V | C28 | U10 pin E2 |
| D14 | Data bus shared with flash and SRAM bit 29 | FSM_D29 | 1.8 V | E23 | U10 pin F2 |
| E12 | Data bus shared with flash and SRAM bit 30 | FSM_D30 | 1.8 V | D23 | U10 pin F1 |
| C15 | Data bus shared with flash and SRAM bit 31 | FSM_D31 | 1.8 V | B28 | U10 pin G1 |
| L13 | Flash address valid | FLASH_ADVn | 1.8 V | C7 | U9 pin F6 |
| K14 | Flash chip enable | FLASH_CEn | 1.8 V | K25 | U9 pin B4 |
| L15 | Flash clock | FLASH_CLK | 1.8 V | K24 | U9 pin E6 |
| M16 | Flash output enable | FLASH_OEn | 1.8 V | K23 | U9 pin F8 |
| L11 | Flash ready/busy | FLASH_RDYBSYn | 1.8 V | L16 | U9 pin F7 |
| M15 | Flash reset | FLASH_RESETn | 1.8 V | E13 | U9 pin D4 |
| L12 | Flash write enable | FLASH_WEn | 1.8 V | L22 | U9 pin G8 |
| N13 | Flash page select | PGM0 | 1.8 V | — | SW3 pin 1 |
| P15 | Flash page select | PGM1 | 1.8 V | — | SW3 pin 2 |
| M14 | Flash page select | PGM2 | 1.8 V | — | SW3 pin 4 |
| N16 | Flash page select | PGM3 | 1.8 V | — | SW3 pin 8 |
| D3 | FPGA configuration complete | FPGA_CONF_DONE | 2.5 V | AH29 | — |
| D3 | FPP configuration data bus bit 0 | FPGA_DATA0 | 2.5 V | T28 | — |
| K4 | FPP configuration data bus bit 1 | FPGA_DATA1 | 2.5 V | T27 | — |
| M2 | FPP configuration data bus bit 2 | FPGA_DATA2 | 2.5 V | R34 | — |
| K3 | FPP configuration data bus bit 3 | FPGA_DATA3 | 2.5 V | R33 | — |
| M2 | FPP configuration data bus bit 4 | FPGA_DATA4 | 2.5 V | T25 | — |

**Table 2–5. MAX II Device Pin-out (Part 5 of 9)**

| MAX II Pin Number | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| L5 | FPP configuration data bus bit 5 | FPGA_DATA5 | 2.5 V | T24 | — |
| M3 | FPP configuration data bus bit 6 | FPGA_DATA6 | 2.5 V | T32 | — |
| L4 | FPP configuration data bus bit 7 | FPGA_DATA7 | 2.5 V | R31 | — |
| C2 | FPP configuration clock | FPGA_DCLK | 2.5 V | AL3 | — |
| E4 | FPGA configuration start | FPGA_NCONFIG | 2.5 V | AE25 | — |
| C3 | FPGA configuration status | FPGA_NSTATUS | 2.5 V | AH28 | — |
| E10 | USB command/data select | USB_CMD_DATA | 2.5 V | Y28 | — |
| B10 | USB empty from MAX II device to Stratix III device | USB_EMPTY | 2.5 V | AH12 | — |
| F9 | USB data from MAX II to Stratix III bit 0 | USB_FD0 | 2.5 V | AE33 | — |
| A9 | USB data from MAX II to Stratix III bit 1 | USB_FD1 | 2.5 V | AE31 | — |
| A8 | USB data from MAX II to Stratix III bit 2 | USB_FD2 | 2.5 V | AC28 | — |
| B8 | USB data from MAX II to Stratix III bit 3 | USB_FD3 | 2.5 V | AA24 | — |
| E8 | USB data from MAX II to Stratix III bit 4 | USB_FD4 | 2.5 V | AF34 | — |
| A7 | USB data from MAX II to Stratix III bit 5 | USB_FD5 | 2.5 V | AG33 | — |
| D8 | USB data from MAX II to Stratix III bit 6 | USB_FD6 | 2.5 V | AA25 | — |
| B7 | USB data from MAX II to Stratix III bit 7 | USB_FD7 | 2.5 V | AE32 | — |
| C9 | USB full from MAX II to Stratix III device | USB_FULL | 2.5 V | AE11 | — |
| J14 | USB clock from MAX II to Stratix III device | USB_IFCLK | 2.5 V | U1 | — |
| A11 | USB read enable from MAX II to Stratix III device | USB_REN | 2.5 V | N5 | — |
| B5 | USB write enable from MAX II to Stratix III device | USB_WEN | 2.5 V | W11 | — |
| L16 | Cypress USB pin multiplexed for I/O or FIFO select | USB_PA5_IF0ADR1 | 2.5 V | — | U12 pin 38 |
| K5 | Cypress USB pin multiplexed for I/O or FIFO packet commit | USB_PA6_PKTEND | 2.5 V | — | U12 pin 39 |
| L2 | Cypress USB pin multiplexed for I/O or gate for other FIFO slaves | USB_PA7_SLCSn | 2.5 V | — | U12 pin 40 |
| C13 | Cypress/FTDI USB data bus bit 0 | USB_PHY_FD0 | 2.5 V | — | U12 pin 18 and U11 pin 25 |
| B16 | Cypress/FTDI USB data bus bit 1 | USB_PHY_FD1 | 2.5 V | — | U12 pin 19 and U11 pin 24 |

**Table 2–5. MAX II Device Pin-out (Part 6 of 9)**

| MAX II Pin Number | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| C12 | Cypress/FTDI USB data bus bit 2 | USB_PHY_FD2 | 2.5 V | — | U12 pin 20 and U11 pin 23 |
| A15 | Cypress/FTDI USB data bus bit 3 | USB_PHY_FD3 | 2.5 V | — | U12 pin 21 and U11 pin 22 |
| D12 | Cypress/FTDI USB data bus bit 4 | USB_PHY_FD4 | 2.5 V | — | U12 pin 22 and U11 pin 21 |
| B14 | Cypress/FTDI USB data bus bit 5 | USB_PHY_FD5 | 2.5 V | — | U12 pin 23 and U11 pin 20 |
| C11 | Cypress/FTDI USB data bus bit 6 | USB_PHY_FD6 | 2.5 V | — | U12 pin 24 and U11 pin 19 |
| B13 | Cypress/FTDI USB data bus bit 7 | USB_PHY_FD7 | 2.5 V | — | U12 pin 25 and U11 pin 18 |
| D11 | Cypress USB data bus bit 8 | USB_PHY_FD8 | 2.5 V | — | U12 pin 45 |
| A13 | Cypress USB data bus bit 9 | USB_PHY_FD9 | 2.5 V | — | U12 pin 46 |
| E11 | Cypress USB data bus bit 10 | USB_PHY_FD10 | 2.5 V | — | U12 pin 47 |
| B12 | Cypress USB data bus bit 11 | USB_PHY_FD11 | 2.5 V | — | U12 pin 48 |
| C10 | Cypress USB data bus bit 12 | USB_PHY_FD12 | 2.5 V | — | U12 pin 49 |
| A12 | Cypress USB data bus bit 13 | USB_PHY_FD13 | 2.5 V | — | U12 pin 50 |
| D10 | Cypress USB data bus bit 14 | USB_PHY_FD14 | 2.5 V | — | U12 pin 51 |
| B11 | Cypress USB data bus bit 15 | USB_PHY_FD15 | 2.5 V | — | U12 pin 52 |
| C7 | Cypress USB clock | USB_PHY_IFCLK | 2.5 V | — | R89 |
| A4 | Cypress USB command/data select | USB_PHY_CMD_DATA | 2.5 V | — | U12 pin 29 |
| E6 | Cypress USB read enable | USB_PHY_REN | 2.5 V | — | U12 pin 30 |
| B4 | Cypress USB write enable | USB_PHY_WEN | 2.5 V | — | U12 pin 31 |
| D6 | Cypress USB empty | USB_PHY_EMPTY | 2.5 V | — | U12 pin 1 |
| C4 | Cypress USB full | USB_PHY_FULL | 2.5 V | — | U12 pin 29 |
| C6 | Cypress USB reset | USB_RESETn | 2.5 V | — | U12 pin 41 |
| B3 | Cypress USB clock out | USB_CLKOUT | 2.5 V | — | U12 pin 54 |
| C5 | Cypress USB wake up | USB_WAKEUP | 2.5 V | — | U12 pin 44 |
| B6 | Cypress USB pin multiplexed for I/O or FIFO select | USB_PA4_IF0ADR0 | 2.5 V | — | U12 pin 37 |
| A2 | Cypress USB pin multiplexed for I/O or 8051 interrupt | USB_PA0_INT0n | 2.5 V | — | U12 pin 33 and U11 pin 14 |
| D5 | Cypress USB pin multiplexed for I/O or 8051 interrupt | USB_PA1_INT1n | 2.5 V | — | U12 pin 34 and U11 pin 12 |
| B1 | Cypress USB pin multiplexed for I/O or output enable for the slave FIFOs. | USB_PA2_SLOE | 2.5 V | — | U12 pin 35 |
| D4 | Cypress USB pin multiplexed for I/O or alternate wake up signal | USB_PA3_WU2 | 2.5 V | — | U12 pin 36 and U11 pin 11 |

**Table 2–5. MAX II Device Pin-out (Part 7 of 9)**

| MAX II Pin Number | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| C8 | FTDI USB read enable | USB_RDn | 2.5 V | — | U11 pin 16 |
| A6 | FTDI USB write enable | USB_WR | 2.5 V | — | U11 pin 15 |
| A5 | FTDI USB reset | USB_RSTn | 2.5 V | — | U11 pin 4 |
| D7 | FTDI USB reset output | USB_RSTOUTn | 2.5 V | — | U11 pin 5 |
| K12 | FTDI USB power enable | USB_PWR_ENn | 1.8 V | — | U11 pin 10 |
| D2 | MAX II output to power seven segment display | PWR_SEG_A | 2.5 V | — | U27 pin 12 |
| E5 | MAX II output to power 7-segment display | PWR_SEG_B | 2.5 V | — | U27 pin 11 |
| D1 | MAX II output to power 7-segment display | PWR_SEG_C | 2.5 V | — | U27 pin 3 |
| F3 | MAX II output to power 7-segment display | PWR_SEG_D | 2.5 V | — | U27 pin 8 |
| E2 | MAX II output to power 7-segment display | PWR_SEG_E | 2.5 V | — | U27 pin 2 |
| F4 | MAX II output to power 7-segment display | PWR_SEG_F | 2.5 V | — | U27 pin 9 |
| E10 | MAX II output to power 7-segment display | PWR_SEG_G | 2.5 V | — | U27 pin 7 |
| F5 | MAX II output to power 7-segment display | PWR_SEG_DP | 2.5 V | — | U27 pin 5 |
| F2 | MAX II output to power 7-segment display | PWR_SEG_MINUS | 2.5 V | — | U27 pin 13 |
| F6 | MAX II output to power 7-segment display | PWR_DIG_SEL1 | 2.5 V | — | U27 pin 1 |
| F1 | MAX II output to power 7-segment display | PWR_DIG_SEL2 | 2.5 V | — | U27 pin 10 |
| G3 | MAX II output to power 7-segment display | PWR_DIG_SEL3 | 2.5 V | — | U27 pin 4 |
| G2 | MAX II output to power 7-segment display | PWR_DIG_SEL4 | 2.5 V | — | U27 pin 6 |
| H5 | Chip select to the power monitor A/D | PMON_CSN | 2.5 V | — | U18 pin 7 |
| J1 | Clock to/from the power monitor A/D | PMON_CLK | 2.5 V | — | U18 pin 9 and U19, pin 19 |
| H4 | Data from the power monitor A/D | PMON_SDI | 2.5 V | — | U18 pin 8 |
| H3 | Data to the power monitor multiplexer | PMON_DATA | 2.5 V | — | U19 pin 19 |
| J2 | Frame synchronization signal to the power monitor multiplexer | PMON_SYNC | 2.5 V | — | U19 pin 17 |
| J16 | Power selection input | PWR_SEL0 | 1.8 V | — | SW6 pin P1 |
| J13 | Power selection input | PWR_SEL1 | 1.8 V | — | SW6 pin P2 |

**Table 2–5. MAX II Device Pin-out (Part 8 of 9)**

| MAX II Pin Number | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| H16 | Power selection input | PWR_SEL2 | 1.8 V | — | SW6 pin P4 |
| H13 | Power selection input | PWR_SEL3 | 1.8 V | — | SW6 pin P8 |
| M4 | JTAG master data input signal | FPGA_JTAG_TDI | 2.5 V | G28 | U2 pin 13 |
| N2 | JTAG master data output | FPGA_JTAG_TDO | 2.5 V | G29 | U2 pin 10 |
| L16 | MAX II chip select | MAX_CSn | 1.8 V | C20 | — |
| P3 | JTAG clock | MAX_JTAG_TCK | 2.5 V | F30 | U3 pin 2 and U2 pin 2 |
| N4 | JTAG mode select | MAX_JTAG_TMS | 2.5 V | — | U3 pin 5, U2 pin 5 |
| K15 | MAX II write enable | MAX_WEn | 1.8 V | G21 | — |
| K13 | MAX II output enable | MAX_OEn | 1.8 V | D20 | — |
| H1 | Connected to Stratix III device | MAX_TO_STRATIX3 | 2.5 V | K1 | — |
| G4 | N/A | MAXGP_JTAG_TCK | 2.5 V | — | U3 pin 3 |
| G1 | N/A | MAXGP_JTAG_TDI | 2.5 V | — | U3 pin 13 |
| G5 | N/A | MAXGP_JTAG_TDO | 2.5 V | — | U3 pin 10 |
| H2 | N/A | MAXGP_JTAG_TMS | 2.5 V | — | U3 pin 6 |
| J4 | Synchronous clock for switching regulators | LT4601_CLK0 | 2.5 V | — | U32 pin A8 |
| K1 | Synchronous clock for switching regulators | LT4601_CLK90 | 2.5 V | — | U33 pin A8 |
| J3 | Synchronous clock for switching regulators | LT4601_CLK180 | 2.5 V | — | U34 pin A8 |
| N3 | JTAG clock | FPGA_JTAG_TCK | 2.5 V | F30 | J18 pin 35 and J8 pin 35 and U2 pin 3 |
| P2 | JTAG mode select | FPGA_JTAG_TMS | 2.5 V | H28 | J18 pin 36 and J8 pin 36 and U2 pin 6 |
| L6 | JTAG data input | MAX_JTAG_TDI | 2.5 V | — | U3 pin 14 and U2 pin 14 |
| M5 | JTAG data output | MAX_JTAG_TDO | 2.5 V | — | U3 pin 11 and U2 pin 11 |
| A10 | Push-button that re-loads the factory default image into the Stratix III device | FACTORY_CONFIGn | 2.5 V | — | S1 |
| B9 | JTAG input to HSMC B | HSMB_JTAG_TDI | 2.5 V | — | J8 pin 38 |
| D9 | JTAG input to HSMC A | HSMA_JTAG_TDI | 2.5 V | — | J18 pin 38 |
| C8 | FTDI USB read enable | USB_RDn | 2.5 V | — | U11 pin 16 |
| A6 | FTDI USB write enable | USB_WR | 2.5 V | — | U11 pin 15 |
| A5 | FTDI USB reset | USB_RSTn | 2.5 V | — | U11 pin 4 |
| D7 | FTDI USB reset output | USB_RSTOUTn | 2.5 V | — | U11 pin 5 |
| K12 | FTDI USB power enable | USB_PWR_ENn | 1.8 V | — | U11 pin 10 |
| J12 | 24 MHz clock input | CLKIN_24 | 1.8 V | — | Y4 pin 3 |
| H12 | 125 MHz clock input | CLKIN_MAX_125 | 1.8 V | — | Y1 pin 4 |

**Table 2–5. MAX II Device Pin-out (Part 9 of 9)**

| MAX II Pin Number | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| G15 | JTAG output from HSMC A | HSMA_JTAG_TDO | 1.8 V | — | J18 pin 37 |
| F15 | JTAG output from HSMC B | HSMB_JTAG_TDO | 1.8 V | — | J8 pin 37 |
| F16 | HSMC A present | HSMA_PSNTn | 1.8 V | — | J18 pin 160 |
| G13 | HSMC B present | HSMB_PSNTn | 1.8 V | — | J8 pin 160 |
| G14 | JTAG control signal | FPGA_BYPASS | 1.8 V | — | SW1 pin 8 |
| E16 | JTAG control signal | HSMA_BYPASS | 1.8 V | — | SW1 pin 7 |
| F11 | JTAG control signal | HSMB_BYPASS | 1.8 V | — | SW1 pin 6 |
| C14 | JTAG control signal | JTAG_SEL | 1.8 V | — | U3 pin 1 and J3 pin 1 |
| M9 | MAX II reset | CPU_RESETn | 1.8 V | AP5 | S6 |
| M8 | MAX II enable | MAX_EN | 1.8 V | — | SW1 pin 5 |
| H15 | MAX II status signal | MAX_ERROR | 1.8 V | — | D34 |
| H14 | MAX II status signal | MAX_LOAD | 1.8 V | — | D33 |
| G16 | MAX II status signal | MAX_FACTORY | 1.8 V | — | D36 |
| G12 | MAX II status signal | MAX_USER | 1.8 V | — | D35 |
| E15 | MAX II status signal | MAX_EMB | 1.8 V | — | D1 |
| E13 | MAX II status signal | DEV_SEL | 1.8 V | — | U2 pin 1 and J2 pin 1 |
| E14 | Control signal | MWATTS_MAMPS | 1.8 V | — | SW2 pin 1 |
| D13 | Control signal | VOLTS_WATTS | 1.8 V | — | SW2 pin 2 |
| R16 | Control signal | RESET_CONFIGn | 1.8 V | — | S7 |
| N14 | PFL enable | MAX_DIP0 | 1.8 V | — | SW2 pin 5 |
| M13 | N/A | MAX_DIP1 | 1.8 V | — | SW2 pin 6 |
| N15 | N/A | MAX_DIP2 | 1.8 V | — | SW2 pin 7 |
| L14 | N/A | MAX_DIP3 | 1.8 V | — | SW2 pin 8 |
| K16 | N/A | MAX_RESERVE0 | 1.8 V | — | SW2 pin 3 |
| J15 | N/A | MAX_RESERVE1 | 1.8 V | — | SW2 pin 4 |
| E7 | N/A | OVERTEMPn | 2.5 V | — | J7 pin 2 |
| N1 | N/A | TSENSE_SMB_DATA | 2.5 V | — | U16 pin 7 |
| L3 | N/A | TSENSE_SMB_CLK | 2.5 V | — | U16 pin 6 |

Table 2–6 lists the MAX II component reference and manufacturing information.

**Table 2–6. MAX II Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U5 | 256-pin device in a BGA package | Altera Corporation | EPM2210GF256C3N | www.altera.com |

# Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements, and is divided into the following groups:

- "Configuration" on page 2–17
  - FPGA programming over USB
  - FPGA programming from flash memory
  - Flash programming over USB
- "Status Elements" on page 2–19
  - Board-specific LEDs
  - Power display
- "Setup Elements" on page 2–21
  - JTAG control DIP switch
  - MAX II device control DIP switch
  - System reset and configuration push-button switches
  - Power Select rotary switch
  - PGM Config Select rotary switch

## Configuration

This section discusses FPGA, flash memory, and MAX II device programming methods supported by the Stratix III development board.

### FPGA Programming Over USB

You can configure the FPGA at any time the board is powered on using the USB 2.0 interface and the Quartus II Programmer in JTAG mode.

The JTAG chain is mastered by the embedded USB-Blaster function found in the MAX II device. Only a USB cable is needed to program the Stratix III FPGA. Any device can be bypassed by using the appropriate switch on the JTAG control DIP switch.

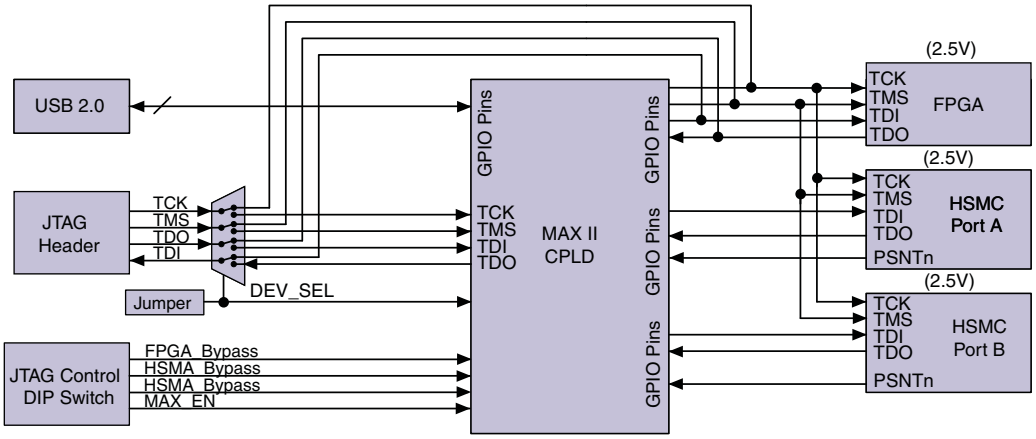
Board reference SW1 position 4 (SW1.4), labeled `MAX_ENABLE` must be in the 0 position for this feature to work properly.

For more information about:

- Advanced JTAG settings, refer to Table 2–7.

- The JTAG control switch, refer to "JTAG Control DIP Switch" on page 2–21.

**Figure 2–6. JTAG Chain with the MAX II Device and the Stratix III Device**




You can use the JTAG header can be used with an external USB-Blaster cable, or equivalent, to program either the MAX II CPLD or the Stratix III FPGA. Most users of the Stratix III development board do not use the JTAG header at all and instead use a USB cable along with the embedded USB-Blaster. Using an external USB-Blaster with the JTAG header requires disabling the embedded USB-Blaster function. See Table 2–7.

If complete repower is required, unplug and replug the USB cable into board reference J5.

**Table 2–7. JTAG Settings (1)**

| Number | Description | FPGA Bypass (SW1.1) | HSMA Bypass (SW1.2) | HSMB Bypass (SW1.3) | MAX Enable (SW1.4) | PFL Enable (SW2.5) (5) | Device Select (DEV_SEL) Jumper, J2 |
|---|---|---|---|---|---|---|---|
| 1 | Embedded USB Blaster (2), (3)<br>Stratix III target device only | 1 | 0 | 0 | 0 | 1 | X |
| 2 | Embedded USB Blaster (2), (3)<br>Stratix III device + HSMC Port A | 1 | 1 | 0 | 0 | 1 | X |
| 3 | Embedded USB Blaster (2), (3)<br>Stratix III device + HSMC Port B | 1 | 0 | 1 | 0 | 1 | X |
| 4 | External USB Blaster (4)<br>Stratix III target device only | X | X | X | 1 | 1 | Off |
| 5 | External USB Blaster (4)<br>MAX II target device only | X | X | X | X | X | On |

**Notes to Table 2–7:**

(1) The nomenclature SW1.1 indicates board reference SW1, position 1.
(2) Requires USB cable plugged into board reference J5.
(3) Board reference SW2.5 might need to be set to off (0) for the embedded USB-Blaster to program the Stratix III FPGA.
(4) Requires external USB-Blaster or equivalent plugged into board reference J23 (PCB bottom).
(5) "1" indicates the PFL is enabled and "0" indicates the PFL is disabled.

### FPGA Programming from Flash Memory

On power-up or after pressing the RESET_CONFIG or FACTORY_CONFIG push-button switch, the MAX II CPLD device's parallel flash loader (PFL) megafunction configures the Stratix III FPGA from flash memory.

The PFL megafunction reads 16-bit data from the flash memory and converts it to passive serial format. The data is written to the Stratix III device's dedicated `DCLK` and `D0` configuration pins at 12 MHz.

You can source the FPGA configuration from flash memory from one of eight images. The image is selected by the PGM Config Select rotary switch, board reference SW3. The rotary switch has 16 positions, but only the first eight are used. The positions correspond to an offset in flash memory where the PFL is directed to for FPGA configuration data.

Board reference SW1 position 4 (SW1.4), labeled `MAX_ENABLE`, must be in the 0 position (off) to enable the configuring from flash memory feature.

### Flash Programming over USB Interface

You can program the flash memory at any time the board is powered up using the USB 2.0 interface and the Quartus II Programmer's JTAG mode.

The development kit implements the Altera PFL megafunction for flash programming. The PFL is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash device. The development kit ships with a pre-built PFL design called **stratixIII_3sl150_dev_pfl**. The PFL design is programmed onto the FPGA whenever the flash is to be written using the Quartus II software.

For more information about:

- The PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.
- Basic flash programming instructions for the development board, refer to *Appendix A: Programming the Flash Device* in the *Stratix III Development Kit User Guide*.

## Status Elements

The development board includes general user, board specific, and HSMC user-defined LEDs. This section discusses board-specific LEDs as well as the power display device. For information about general and HSMC user-defined LEDS, refer to "User-Defined LEDs" on page 2–30.

## Board Specific LEDs

There are 18 board-specific, factory-designated LEDs. Table 2–8 lists the LED board references, names, and descriptions.

**Table 2–8. Board-Specific LEDs**

| Board Reference | LED Name | Description |
|---|---|---|
| D16 | Power | Illuminates when board power switch SW4 is on.<br>(Requires 14 V to 20 V input to DC input jack J2) |
| D32 | CONF DONE | Illuminates when FPGA is successfully configured. Driven by Stratix III FPGA. |
| D33 | Loading | Illuminates when MAX II CPLD is actively configuring the FPGA. Driven by the MAX II CPLD. |
| D34 | Error | Illuminates when MAX II CPLD fails to successfully configure the FPGA. Driven by the MAX II CPLD. |
| D36 | Factory | Illuminates when FPGA is configured with the default factory FPGA design. Driven by the MAX II CPLD. |
| D35 | User | Illuminates when FPGA is configured with a design other than the default factory FPGA design. Driven by the MAX II CPLD. |
| D14 | ENET TX | Illuminates when transmit data is active from the Ethernet PHY. Driven by the Marvell 88E1111 PHY. |
| D15 | ENET RX | Illuminates when receive data is active from the Ethernet PHY. Driven by the Marvell 88E1111 PHY. |
| D6 | 10 MBytes | Illuminates when Ethernet PHY is using the 10-Mbps connection speed. Driven by the Marvell 88E1111 PHY. |
| D7 | 100 MBytes | Illuminates when Ethernet PHY is using the 100-Mbps connection speed. Driven by the Marvell 88E1111 PHY. |
| D8 | 1000 MBytes | Illuminates when Ethernet PHY is using the 1000-Mbps connection speed. Driven by the Marvell 88E1111 PHY. Also connects to Stratix III FPGA. |
| D9 | Duplex | Illuminates when Ethernet PHY is both sending and receiving data. Driven by the Marvell 88E1111 PHY. |
| D17 | HSMC Port A present | Illuminates when HSMC Port A has a board or cable attached that grounds pin 160. |
| D10 | HSMC Port B present | Illuminates when HSMC Port B has a board or cable attached that grounds pin 160. |
| D2 | HSMC Port B TX | Illuminates when transmit data is active from the HSMC. Driven by the Stratix III device. |
| D3 | HSMC Port B RX | Illuminates when receive data is active from the HSMC. Driven by the Stratix III device. |
| D11 | HSMC Port A TX | Illuminates when transmit data is active from the HSMC. Driven by the Stratix III device. |
| D12 | HSMC Port A RX | Illuminates when receive data is active from the HSMC. Driven by the Stratix III device. |

Table 2–9 lists the board-specific LEDs component reference and manufacturing information.

**Table 2–9. Board-Specific LEDs Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| D2, D3, D6 – D12, D14, D15, D17, D32, D33, D35, D36 | Green LED, 1206, SMT, clear lens, 2.1 V | Lumex, Inc. | SML-LX1206GC-TR | www.lumex.com |
| D16 | Blue LED, 1206, SMT, clear lens, 3.5 V | Lumex, Inc. | SML-LX1206USBC-TR | www.lumex.com |
| D34 | Red LED, 1206, SMT, clear lens, 2.0 V | Lumex, Inc. | SML-LX1206IC-TR | www.lumex.com |

### Power Display

The power being measured by the MAX II CPLD and associated A/D is displayed on a dedicated 7-segment display connected to the MAX II device called *Power Display*.

## Setup Elements

The development board includes user, JTAG control, and board-specific DIP switches; system reset and configuration push-button switches; and rotary switches. This section discusses the following items:

- JTAG control DIP switch
- MAX II device control DIP switch
- System reset and configuration push-buttons
- Power Select rotary switch
- PGM Config Select rotary switch

### JTAG Control DIP Switch

Board reference SW1 is a four-position JTAG control DIP switch, provided to either remove or include devices in the active JTAG chain. Additionally, the JTAG control DIP switch is also used to disable the embedded USB-Blaster cable when using an external USB-Blaster cable. Table 2–10 lists the switch position, name, and description.

**Table 2–10. JTAG Control DIP Switch Signal Names and Descriptions (Part 1 of 2)**

| DIP Switch | Signal Name | Description |
|---|---|---|
| 1 | FPGA_BYPASS | 1 = FPGA in JTAG chain<br>0 = FPGA not in JTAG chain |
| 2 | HSMA_BYPASS | 1 = HSMC Port A in JTAG chain (only if installed)<br>0 = HSMC Port A not in JTAG chain |

**Table 2–10. JTAG Control DIP Switch Signal Names and Descriptions (Part 2 of 2)**

| DIP Switch | Signal Name | Description |
|---|---|---|
| 3 | HSMB_BYPASS | 1 = HSMC Port B in JTAG chain (only if installed)<br>0 = HSMC Port B not in JTAG chain |
| 4 | MAX_ENABLE | 1 = MAX II device disabled<br>0 = MAX II device enabled |

Because the JTAG chain also contains the two HSMC interface connectors, the SW1 DIP switch allows data to bypass the HSMC interfaces as well as the MAX II CPLD. See "FPGA Programming Over USB" on page 2–17. For information about user-defined DIP switches, refer to "User-Defined DIP Switches" on page 2–29.

Table 2–11 lists the JTAG control switch component reference and manufacturing information.

**Table 2–11. JTAG Control Switch Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number |
|---|---|---|---|
| SW1 | Four-position slider DIP switch | C&K Components ITT Industries | TDA04H0SB1 |

## MAX II Device Control DIP Switch

Board reference SW2 is the MAX II device control DIP switch, which controls various features specific to the Stratix III development board. Table 2–12 lists the switch position, name, and description.

**Table 2–12. MAX II Device Control DIP Switch Position, Name, and Description**

| Switch | Name | Description |
|---|---|---|
| 8 | MAX_DIP3 | Reserved |
| 7 | MAX_DIP2 | Reserved |
| 6 | MAX_DIP1 | Reserved |
| 5 | MAX_DIP0 | 1 = MAX II device PFL enabled, 0 = MAX II device PFL disabled |
| 4 | RESERVE1 | Reserved |
| 3 | RESERVE0 | Reserved |
| 2 | VOLTS_WATTS | 1 = power display shows mW/mA, 0 = power display shows voltage |
| 1 | MWATTS_MAMPS | 1 = power display shows mA, 0 = power display shows mW |

Table 2–13 lists the MAX II device control DIP switch component reference and manufacturing information.

**Table 2–13. MAX II Device Control DIP Switch Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| SW2 | 8-position rocker DIP switch | Grayhill Corporation | 76SB08ST | www.grayhill.com |

## System Reset and Configuration Switches

Board reference S7 is the system reset push-button switch, RESET_CONFIG, which is an input to the MAX II device. This switch forces a reconfiguration of the FPGA from flash memory. The location in flash memory is based on the input from the PGM Config Select rotary switch position for the signals PGM [2:0]. The MAX II device uses the RESET_CONFIGn pin as its reset along with the CPU_RESET pin push-button.

Board reference S6 is the CPU reset push-button switch, CPU_RESET, which is an input to both the Stratix III FPGA and the MAX II CPLD. The CPU_RESET push-button is intended to be the master reset signal for the FPGA design loaded in the Stratix III device, and connects to a regular I/O pin on the FPGA. The MAX II device uses this push-button as its reset along with the RESET_CONFIG and FACTORY_CONFIG push-buttons.

Board reference S1 is the factory push-button, FACTORY_CONFIG, which is an input to the MAX II device. The FACTORY_CONFIG pin forces a reconfiguration of the FPGA with the factory default FPGA design, which is located at the base of flash memory. See Table 2–14.

**Table 2–14. Push-Button Switch Signal Name and Function**

| Board Reference | Schematic Signal Name | Stratix III Device Pin Number | MAX II Device Pin Number |
|---|---|---|---|
| S1 | FACTORY_CONFIG | — | A10 |
| S7 | RESET_CONFIGn | — | R16 |
| S6 | CPU_RESET | T21 | M9 |

Table 2–15 lists the push-button switch component reference and manufacturing information.

**Table 2–15. Push-Button Switch Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| S1, S6, S7 | Push-button switch | Panasonic | EVQAPAC07K | www.panasonic.com |

For information about user-defined push-buttons, refer to "User-Defined Push-Button Switches" on page 2–28.

## Power Select Rotary Switch

A 16-position rotary switch, board reference SW6, is used to select the current power rail whose power is being measured and displayed on the power display. The rotary switch is connected to the MAX II CPLD.

Upon first use, after configuring or powering up the board, make sure you initiate changes to the rotary switch (SW6) so that the measurement circuit can initiate a channel reading. Otherwise, the measurement might be reading a previous capture.

Table 2–16 lists the Power Select rotary switch number, name, power pin, and description.

**Table 2–16. Power Select Rotary Switch Number, Name, Pin, and Description**

| Number | Schematic Signal Name | Power Pin Name | Description |
|---|---|---|---|
| 0 | VCCL | VCCL | FPGA core voltage power |
| 1 | 1.1V_VCC | VCC | FPGA I/O registers power |
| 2 | 2.5V_A | VCCA, VCCPT | FPGA analog power, programmable power technology |
| 3 | 2.5V_VCCPD | VCCPD | FPGA I/O pre-driver power |
| 4 | 2.5V_VCCPGM | VCCPGM | FPGA configuration pins power |
| 5 | — | — | — |
| 6 | 1.8 V_S3 | VCCIO 1A, 1C, 3A, 3B, 3C, 4B, 4C, 8A, 8B, 8C | FPGA I/O power banks 1A, 1C, 3A, 3B, 3C, 4B, 4C, 8A, 8B, 8C |
| 7 | 2.5V_B2 | VCCIO 2A, 2C | FPGA I/O power banks 2A, 2C |
| 8 | 2.5V_B4A_B5_B6 | VCCIO 4A, 5A, 5C, 6A, 6C | FPGA I/O power banks 4A, 5A, 5C, 6A, 6C |
| 9 | 1.5V_1.8V_B7 | VCCIO 7A, 7B, 7C | FPGA I/O power banks 7A,7B,7C |
| 10 | — | — | — |
| 11 | — | — | — |
| 12 | — | — | — |
| 13 | — | — | — |
| 14 | — | — | — |
| 15 | — | — | — |

Table 2–17 lists Power Select rotary switch component reference and manufacturing information.

**Table 2–17. Power Select Rotary Switch Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| SW6 | 16-position rotary switch | Grayhill Corporation | 94HCB16WT | www.grayhill.com |

## PGM Config Select Rotary Switch

A 16-position rotary switch, board reference SW3, is used to set the location in flash memory from which the Stratix III FPGA design is loaded. The rotary switch has 16 positions but only the first eight are used.

For information about the flash memory locations, refer to "Flash Memory" on page 2–63.

Table 2–18 lists PGM Config Select rotary switch component reference and manufacturing information.

**Table 2–18. PGM Config Select Rotary Switch Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| SW3 | Rotary switch | Grayhill Corporation | 94HCB16WT | www.grayhill.com |

# Clocking Circuitry

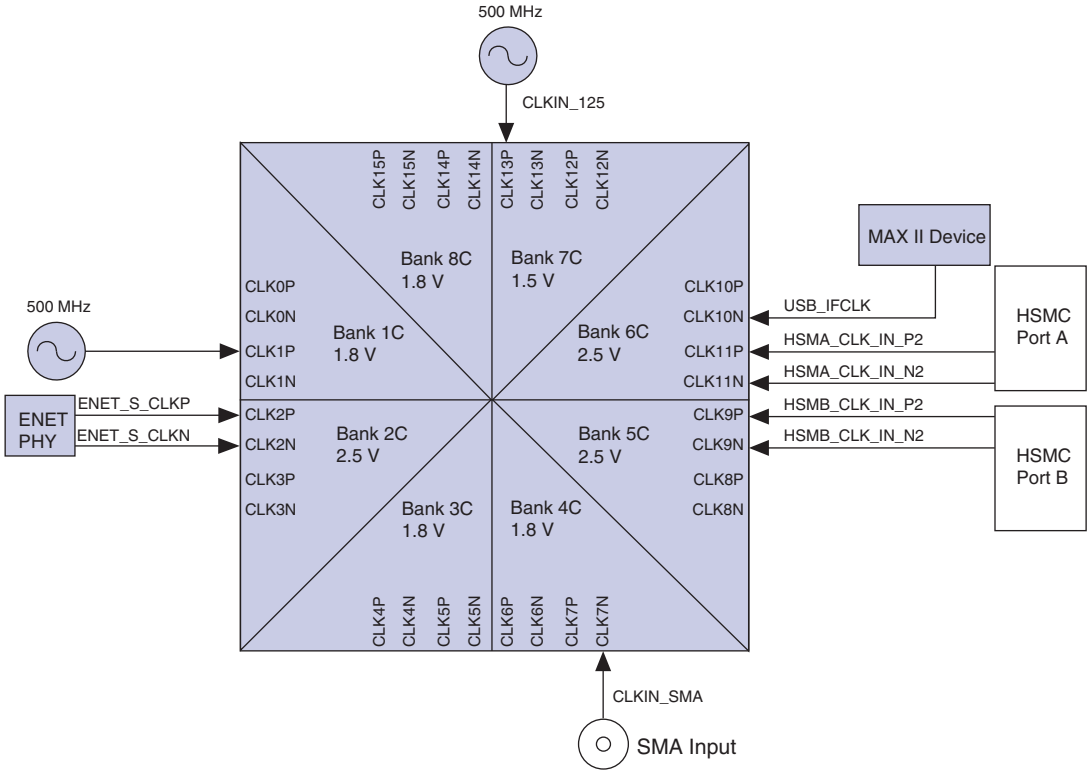
This section describes the Stratix III FPGA clocking inputs and outputs. The clocking block comprises the following items:

- High-speed clock oscillators:
  - 50-MHz, FPGA PLL input
  - 125-MHz FPGA PLL input
  - 125-MHz MAX II CPLD input
  - 24-MHz MAX II CPLD input
- Reference clocks:
  - 6-MHz USB PHY reference clock (FTDI device)
  - 24-MHz USB PHY reference clock (Cypress device)
  - 25-MHz Ethernet PHY reference clock
- SMA connectors for clocking input and output signals

## Stratix III FPGA Clock Inputs

Figure 2–7 outlines the inputs from the Stratix III FPGA. All PLL inputs are located in the C sub-bank of each device bank. The clocks are sourced by the on-board oscillators, SMA connectors, Ethernet, MAX II CPLD, and HSMC ports.

**Figure 2–7. Stratix III FPGA Clock Inputs**



## Stratix III FPGA Clock Outputs

Figure 2–8 outlines the outputs from the Stratix III FPGA. Most of the output clocks originate from the regular I/O pins (non-PLL pins). These clocks drive each of the interfaces on the Stratix III development board.

**Figure 2–8. Stratix III FPGA Clock Outputs**

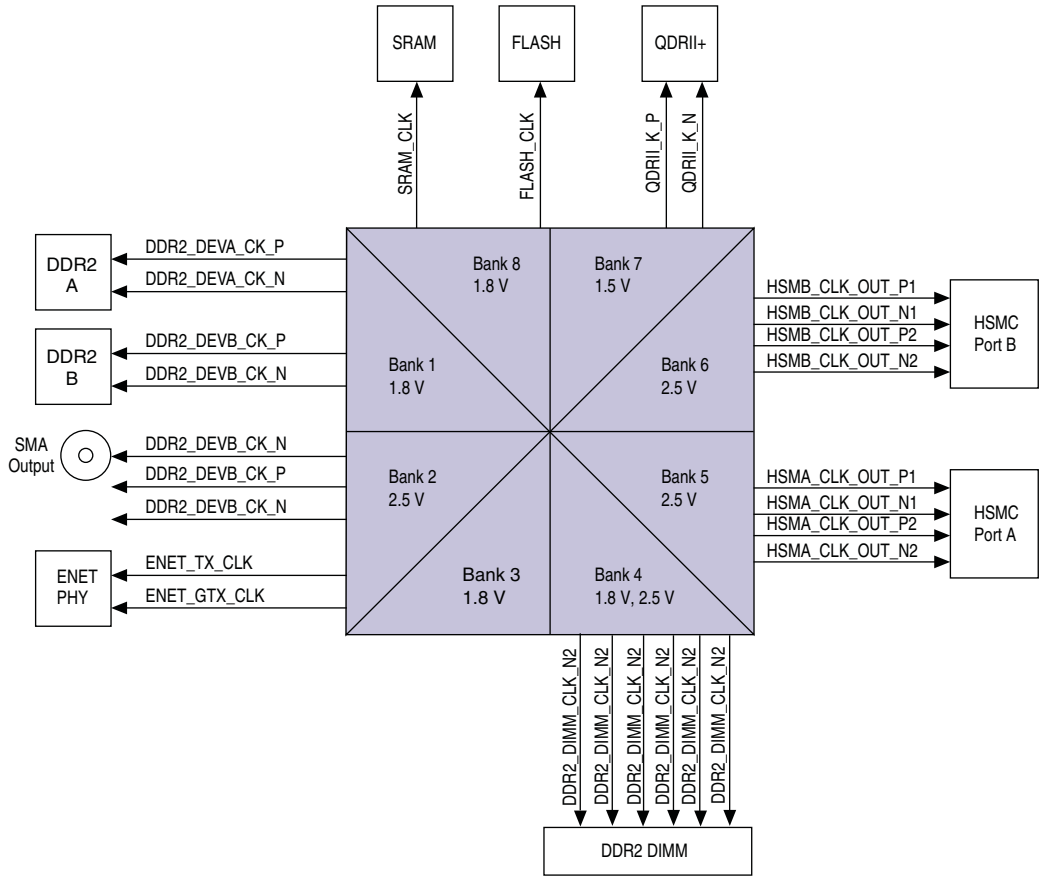



Table 2–19 shows the clocking parts list.

**Table 2–19. Stratix III Development Board Clocking Parts List**

| Board Reference | Description | Manufacturer | Manufacturer Part Number | Manufacturer Website |
|---|---|---|---|---|
| Y6 | 50-MHz LVDS oscillator | Pletronics | SM5545TEX-50.00M | www.pletronics.com |
| Y1,Y5 | 125-MHz LVDS oscillator | Pletronics | SM5545TEX-125.00M | www.pletronics.com |
| J16, J17 | SMA for external clock input/output | Lighthorse Technologies | LTI-SASF546-P26-X1 | www.rfconnector.com |
| Y2 | 24-MHz crystal | Abracon Corporation | ABL-24.000MHZ-12 | www.abracon.com |
| Y3 | 6-MHz crystal | Abracon Corporation | ABL-6.000MHZ-B2 | www.abracon.com |
| X1 | 25-MHz crystal oscillator | ECS, Inc. | ECS-3953C-250-B | www.ecsxtal.com |
| Y4 | 24-MHz crystal oscillator | Pletronics | SM5545TEX-24.00M | www.pletronics.com |

Table 2–20 lists the board's clock distribution system.

**Table 2–20. Stratix III Development Board Clock Distribution**

| Source | Schematic Signal Name | I/O Standard | Signal Originates From | Signal Propagates To |
|---|---|---|---|---|
| 125-MHz (Y5) oscillator | clkin_125 | Input | Y5 | Stratix III device pin B16 |
| 50-MHz (Y6) oscillator | clkin_50 | Input | Y6 | Stratix III device pin T33 |
| User input (SMA clock input) | clkin_sma | Input | J16 | Stratix III device pin AP15 |
| User output (SMA clock output) | clkout_sma | Output | J17 | From Stratix III device pin AE27 |
| 25 MHz (reference clock)<br>This clock can change both speed and direction depending on the Ethernet link speed (10/100/1000) | enet_rx_clk | Input | U25 | Stratix III device pin AK28 |
| 24-MHz (Y4) oscillator | clkin_24 | Input | Y4 | MAX II device pin J12 (Bank 3) |
| 6-MHz crystal | XTIN/XTOUT | Input | Y3 | FTDI USB PHY |
| 24-MHz crystal | XTALIN/XTALOUT | Input | Y2 | Cypress USB PHY |
| 125-MHz (Y1) oscillator | clkin_max_125 | Input | Y1 | MAX II device pin H12 (Bank 3) |

For more information about the board's clocking scheme, refer to the Stratix III development board schematics included with the Stratix III development board kit.

# General User Interfaces

To allow you to fully leverage the I/O capabilities of the Stratix III device for debugging, control, and monitoring purposes, the following general user interfaces are available on the board:

- "User-Defined Push-Button Switches" on page 2–28
- "User-Defined DIP Switches" on page 2–29
- "User-Defined LEDs" on page 2–30
- "7-Segment Displays" on page 2–31
- "LCD Displays" on page 2–33
- "Speaker Header" on page 2–38

## User-Defined Push-Button Switches

The development board includes four general user and one user reset push-button. For information about the system and reset push-button switches, refer to "System Reset and Configuration Switches" on page 2–23.

Board references S2 through S5 are push-button switches allowing user interactions with the Stratix III device. When the switch is pressed and held down, the device pin is set to a logic 0; when the switch is released, the device pin is set to a logic 1. There is no board-specific function for these four push-button switches.

Board reference S6 is the user reset push-button switch, CPU_RESET, which is an input to both the Stratix III device and MAX II CPLD. The CPU_RESET is intended to be the master reset signal for the FPGA design loaded into the Stratix III device. Still, the CPU_RESET is also a regular I/O pin. The MAX II device uses the DEV_CLR pin as its reset along with the RESET_CONFIG push-button switch.

Table 2–21 lists the schematic signal names and corresponding Stratix III pin numbers.

**Table 2–21. User Push-Button Switch Signal Names and Functions**

| Board Reference | Description | Schematic Signal Name | Stratix III Device Pin Number | Other Connections |
|---|---|---|---|---|
| S2 | User-defined push-button | USER_PB3 | K17 | — |
| S3 | User-defined push-button | USER_PB2 | A16 | — |
| S4 | User-defined push-button | USER_PB1 | A17 | — |
| S5 | User-defined push-button | USER_PB0 | B17 | — |
| S6 | User-defined push-button | CPU_RESET | AP5 | U5 pin M9 |

**Note to Table 2–21:**

(1) The pull-up resistors for the push-buttons are connected to 2.5 V. The inputs pads on the FPGA can accept an input voltage up to the maximum input voltage for the device. The logic threshold is determined by the VCCIO of the bank and the selected I/O configuration.

Table 2–22 lists the push-button switch component reference and manufacturing information.

**Table 2–22. Push-Button Switch Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| S2 through S6 | Push-button switch | Panasonic | EVQPAC07K | www.panasonic.com |

## User-Defined DIP Switches

Board reference SW5 is an 8-pin DIP switch. The switches in SW5 are user-defined, and are provided for additional FPGA input control. Each pin can be set to a logic 1 by pushing it to the open position, and each pin can be set to a logic 0 by pushing it to the closed position. There is no board-specific function for these switches.

Table 2–23 lists the user DIP switch settings, schematic signal name, and corresponding Stratix III device's pin number.

**Table 2–23. User-Defined DIP Switch Pin-Out (SW5) (Part 1 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Device Pin Number |
|---|---|---|---|---|
| SW5 pin1 | User-defined DIP switch pin 1 | USER_DIPSW0 | 1.8 V | B19 |
| SW5 pin 2 | User-defined DIP switch pin 2 | USER_DIPSW1 | 1.8 V | A19 |
| SW5 pin 3 | User-defined DIP switch pin 3 | USER_DIPSW2 | 1.8 V | C18 |
| SW5 pin 4 | User-defined DIP switch pin 4 | USER_DIPSW3 | 1.8 V | A20 |
| SW5 pin 5 | User-defined DIP switch pin 5 | USER_DIPSW4 | 1.8 V | K19 |
| SW5 pin 6 | User-defined DIP switch pin 6 | USER_DIPSW5 | 1.8 V | J19 |

**Table 2–23. User-Defined DIP Switch Pin-Out (SW5) (Part 2 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Device Pin Number |
|---|---|---|---|---|
| SW5 pin 7 | User-defined DIP switch pin 7 | USER_DIPSW6 | 1.8 V | L19 |
| SW5 pin 8 | User-defined DIP switch pin 8 | USER_DIPSW7 | 1.8 V | L20 |

Table 2–24 lists the user-defined DIP switch component reference and manufacturing information.

**Table 2–24. User-Defined DIP Switch Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| SW5 | 8-position rocker DIP switch | Grayhill Corporation | 76SB08ST | www.grayhill.com |

## User-Defined LEDs

The board includes general and HSMC user-defined LEDs. This section discusses all user-defined LEDs. For information about board specific or status LEDs, refer to "Status Elements" on page 2–19.

### General User-Defined LEDs

Board references D20 through D27 are eight user LEDs, which allow status and debugging signals to be driven to LEDs from the FPGA designs loaded into the Stratix III device. The LEDs illuminate when a logic 0 is driven, and do not illuminate when a logic 1 is driven. There is no board-specific function for these LEDs.

Table 2–25 lists the general user LED reference number, schematic signal name, and corresponding Stratix III device pin number.

**Table 2–25. LED Reference Number, Schematic Signal Name, and Stratix III Device Pin Number**

| LED Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Device Pin Number |
|---|---|---|---|---|
| D27 | User-defined LED | USER_LED0 | 1.8 V | F21 |
| D26 | User-defined LED | USER_LED1 | 1.8 V | C23 |
| D25 | User-defined LED | USER_LED2 | 1.8 V | B23 |
| D24 | User-defined LED | USER_LED3 | 1.8 V | A23 |
| D23 | User-defined LED | USER_LED4 | 1.8 V | D19 |
| D22 | User-defined LED | USER_LED5 | 1.8 V | C19 |
| D21 | User-defined LED | USER_LED6 | 1.8 V | F19 |
| D20 | User-defined LED | USER_LED7 | 1.8 V | E19 |

Table 2–26 lists the general user-defined LED component reference and manufacturing information.

**Table 2–26. General User-Defined LED Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| D20-D27 | Green LEDs, 1206, SMT, clear lens, 2.1 V | Lumex, Inc. | SML-LX1206GC-TR | www.lumex.com |

### HSMC User-Defined LEDs

The HSMC cards Port A and Port B have two LEDs located nearby. There are no board-specific functions for the HSMC LEDs; however, the LEDs are labeled *TX* and *RX*, and are intended to display data flow to and from connected HSMC cards. The LEDs are driven by the Stratix III device.

Table 2–27 lists the HSMC user-defined LED board reference number, schematic signal name, and corresponding Stratix III device pin number.

**Table 2–27. HSMC User-Defined LEDs**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Device Pin Number |
|---|---|---|---|---|
| D11 | User-defined LED, but labeled *TX* in silk-screen for HSMC Port A. | HSMA_TX_LED | 1.8 V | AG29 |
| D12 | User-defined LED, but labeled *RX* in silk-screen for HSMC Port A. | HSMA_RX_LED | 1.8 V | Y25 |
| D2 | User-defined LED, but labeled *TX* in silk-screen for HSMC Port B. | HSMA_TX_LED | 1.8 V | AG34 |
| D3 | User-defined LED, but labeled *RX* in silk-screen for HSMC Port B. | HSMA_RX_LED | 1.8 V | AJ12 |

Table 2–28 lists the HSMC user-defined LED component reference and manufacturing information.

**Table 2–28. HSMC User-Defined LED Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| D2, D3, D11, D12 | Green LED, 1206, SMT, clear lens, 2.1 V | Lumex, Inc. | SML-LX1206GC-TR | www.lumex.com |

## 7-Segment Displays

This section discusses the following two on-board displays:

- User 7-segment display
- Power 7-segment display

## User 7-Segment Display

Board reference U28 is a four-digit, user-defined, 7-segment display that is labeled *User Display*. Each segment's LED driver input signals are multiplexed to each of the four digits and a minus sign. Table 2–29 lists the 7-segment display pin-out.

**Table 2–29. User-Defined 7-Segment Display Pin-Out**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Device Pin Name |
|---|---|---|---|---|
| U28 pin 12 | User-defined display signal | SEVEN_SEG_A | 2.5 V | AE10 |
| U28 pin 11 | User-defined display signal | SEVEN_SEG_B | 2.5 V | AL5 |
| U28 pin 3 | User-defined display signal | SEVEN_SEG_C | 2.5 V | AC12 |
| U28 pin 8 | User-defined display signal | SEVEN_SEG_D | 2.5 V | AM5 |
| U28 pin 9 | User-defined display signal | SEVEN_SEG_E | 2.5 V | AF11 |
| U28 pin 7 | User-defined display signal | SEVEN_SEG_F | 2.5 V | AM6 |
| U28 pin 5 | User-defined display signal | SEVEN_SEG_G | 2.5 V | AP3 |
| U28 pin 2 | User-defined display signal | SEVEN_SEG_DP | 2.5 V | AK6 |
| U28 pin 13 | User-defined display signal | SEVEN_SEG_MINUS | 2.5 V | AH11 |
| U28 pin 1 | User-defined display select signal | SEVEN_SEG_SEL1 | 2.5 V | AM4 |
| U28 pin 10 | User-defined display select signal | SEVEN_SEG_SEL2 | 2.5 V | AE12 |
| U28 pin 4 | User-defined display select signal | SEVEN_SEG_SEL3 | 2.5 V | AL4 |
| U28 pin 6 | User-defined display select signal | SEVEN_SEG_SEL4 | 2.5 V | AH8 |

The four-pin, 7-segment display uses fewer pins than 2-digit, 7-segment displays. See Figure 2–9.

**Figure 2–9. 7-Segment Display**

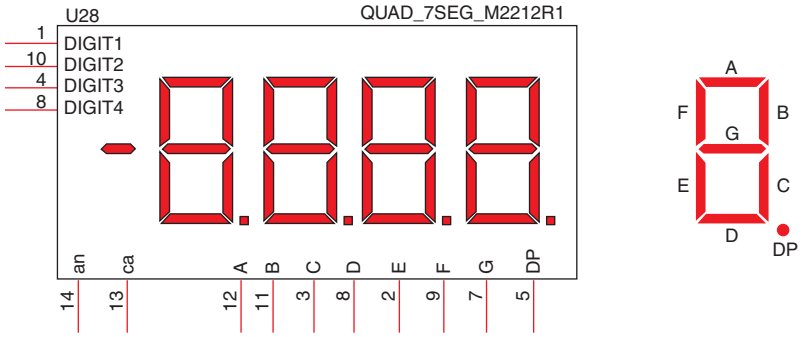



Table 2–30 lists the 7-segment display component reference and manufacturing information.

**Table 2–30. 7-Segment Display Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U28 | 7-segment, green LED display | Lumex, Inc. | LDQ-M2212R1 | www.lumex.com |

### Power 7-Segment Display

The power measured by the MAX II CPLD and associated A/D is displayed on board reference U27, which is a dedicated 7-segment display connected to the MAX II CPLD, labeled *Power Display*.

Table 2–31 lists the power 7-segment display component reference and manufacturing information.

**Table 2–31. Power 7-Segment Display Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U27 | 7-segment, green LED display | Lumex, Inc. | LDQ-M2212R1 | www.lumex.com |

## LCD Displays

The development board accommodates two LCD displays:

- Character LCD
- Graphics LCD

The character display is a 16-character, by 2-line LCD display. The graphics is a 128 × 64 pixel transmissive graphics LCD. The two displays have separate buses. This section describes both displays.

### Character LCD

The board contains a single 14-pin 0.1 in. pitch dual-row header, used to interface to a 16-character by 2-line LCD display, manufactured by Lumex (part number LCM-S01602DSR/C). The LCD has a 14-pin receptacle that mounts directly to the board's 14-pin header, so it can be easily removed for access to components under the display—or to use the header for debugging or other purposes.

Table 2–32 summarizes the character LCD interface pins. Signal name and direction are relative to the Stratix III FPGA. For functional descriptions, see Table 2–33.

**Table 2–32. Character LCD (J22) Header I/O**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J22 pin 7 | LCD data bus bit 0 | LCD_DATA0 | 2.5 V | AJ8 |
| J22 pin 8 | LCD data bus bit 1 | LCD_DATA1 | 2.5 V | AJ6 |
| J22 pin 9 | LCD data bus bit 2 | LCD_DATA2 | 2.5 V | AD13 |
| J22 pin 10 | LCD data bus bit 3 | LCD_DATA3 | 2.5 V | AJ7 |
| J22 pin 11 | LCD data bus bit 4 | LCD_DATA4 | 2.5 V | AF10 |
| J22 pin 12 | LCD data bus bit 5 | LCD_DATA5 | 2.5 V | AN6 |
| J22 pin 13 | LCD data bus bit 6 | LCD_DATA6 | 2.5 V | AN3 |
| J22 pin 14 | LCD data bus bit 7 | LCD_DATA7 | 2.5 V | AK7 |
| J22 pin 4 | LCD data/command select | LCD_D_Cn | 2.5 V | AP2 |
| J22 pin 5 | LCD write enable | LCD_WEn | 2.5 V | AL8 |
| J22 pin 6 | LCD chip select | LCD_CSn | 2.5 V | AD12 |

Table 2–33 shows pin definitions, and is an excerpt from the Lumex data sheet.

For more information such as timing, character maps, interface guidelines, and related documentation, visit www.lumex.com.

**Table 2–33. Character LCD Display Pin Definitions**

| Pin Number | Symbol | Level | Function | |
|---|---|---|---|---|
| 1 | $V_{DD}$ | — | Power supply | 5 V |
| 2 | $V_{SS}$ | — | | GND (0V) |
| 3 | $V_0$ | — | | For LCD drive |
| 4 | RS | H/L | Register select signal<br>H: Data input<br>L: Instruction input | |
| 5 | R/W | H/L | H: Data read (module to MPU)<br>L: Data write (MPU to module) | |
| 6 | E | H, H to L | Enable | |
| 7~14 | DB0~DB7 | H/L | Data bus, software selectable 4- or 8-bit mode | |

Figure 2–10 shows a functional block diagram of the Lumex LCD display device.

The particular model used does not have a backlight and the LCD drive pin is not connected.

**Figure 2–10. LCD Display Block Diagram**

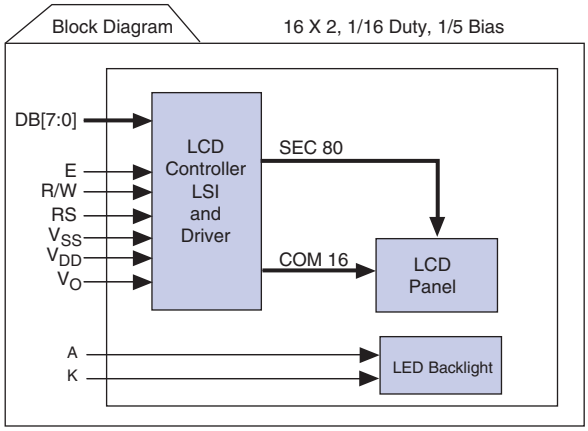


Figure 2–11 shows a mechanical diagram of the LCD display. The 14-pin receptacle mounts underneath the display in the holes to the left.

**Figure 2–11. LCD Display Dimensions**

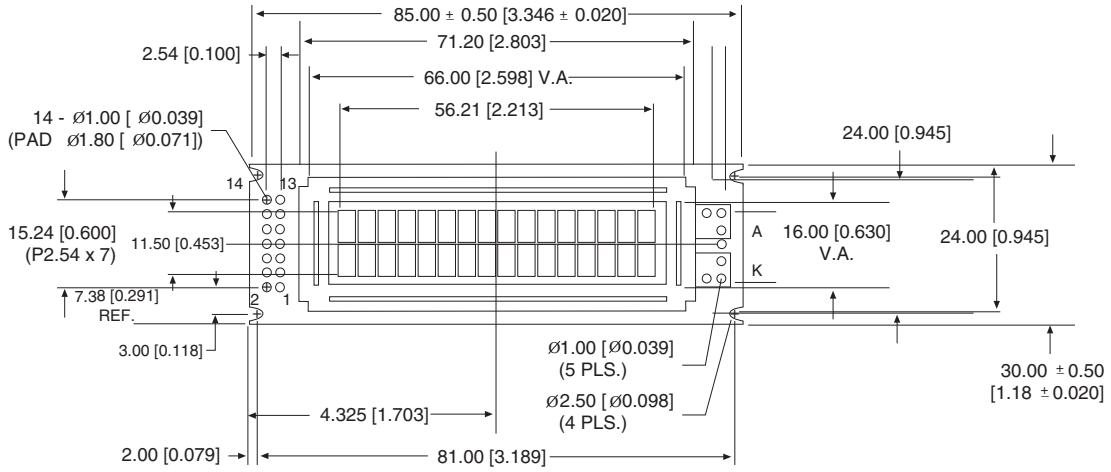



Table 2–34 lists the character LCD display component reference and manufacturing information.

**Table 2–34. Character LCD Display Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| J22 | 2 × 7 pin, 100 mil, vertical header | Samtec | TSM-107-01-G-DV | www.samtec.com |
| | 2 × 16 character display, 5 × 8 dot matrix | Lumex Inc. | LCM-S01602DSR/C | www.lumex.com |

## Graphics LCD

The board contains a 30-pin, fine-pitch connector to interface directly to a 128 × 64 dot matrix graphics LCD display via a flex-cable that is soldered to the display itself. The display is an Optrex, part number F-51852GNFQJ-LB-AIN (blue pixels) or F-51852GNFQJ-LB-CAN (green pixels). The pin-out of this interface connector is compatible with a variety of displays.

For the graphics LCD data sheet and related documentation, visit www.optrex.com.

Table 2–35 lists the graphics LCD pin name, description, and type. Signal name and direction are relative to the Stratix III FPGA.

**Table 2–35. Graphics LCD Header (J24) (Part 1 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J24 pin 6 | LCD data bus bit 0 | OLED_DATA0 | 2.5 V | AB31 |
| J24 pin 7 | LCD data bus bit 1 | OLED_DATA1 | 2.5 V | AG32 |
| J24 pin 8 | LCD data bus bit 2 | OLED_DATA2 | 2.5 V | AB27 |
| J24 pin 9 | LCD data bus bit 3 | OLED_DATA3 | 2.5 V | AC32 |

**Table 2–35. Graphics LCD Header (J24) (Part 2 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J24 pin 10 | LCD data bus bit 4 | OLED_DATA4 | 2.5 V | AL32 |
| J24 pin 11 | LCD data bus bit 5 | OLED_DATA5 | 2.5 V | AB30 |
| J24 pin 12 | LCD data bus bit 6 (or SCLK) | OLED_DATA6 | 2.5 V | AC26 |
| J24 pin 13 | LCD data bus bit 7 (or SDATA) | OLED_DATA7 | 2.5 V | AA30 |
| J24 pin 28 | Parallel interface selection (high = 68 series, low = 80 series) | OLED_BS1 | 2.5 V | Y26 |
| J24 pin 1 | LCD chip select | OLED_CSn | 2.5 V | AE30 |
| J24 pin 3 | LCD data/command select | OLED_D_Cn | 2.5 V | AD26 |
| J24 pin 5 | LCD read enable | OLED_E_RDn | 2.5 V | AG31 |
| J24 pin 2 | LCD reset | OLED_RSTn | 2.5 V | AP4 |
| J24 pin 29 | LCD parallel/serial data select | OLED_SERn | 2.5 V | AA27 |
| J24 pin 4 | LCD write enable | OLED_WEn | 2.5 V | AA31 |

For more information about the data sheet and related documentation, visit Lumex at www.lumex.com.

Board defaults graphics LCD interface to 80 series CPU mode and parallel interface. You can modify these defaults by writing to the appropriate register in the MAX II CPLD using the FSM bus.

Figure 2–12 is an excerpt from the Optrex data sheet showing the control chip in the LCD module and illustrates the functional block diagram of the display driver. The control chip is from New Japan Radio Corporation, part number NJU6676.

For more information, contact Optrex America at www.optrex.com or New Japan Radio at www.njr.co.jp.

**Figure 2–12. Graphics LCD Functional Block Diagram of Display Driver**

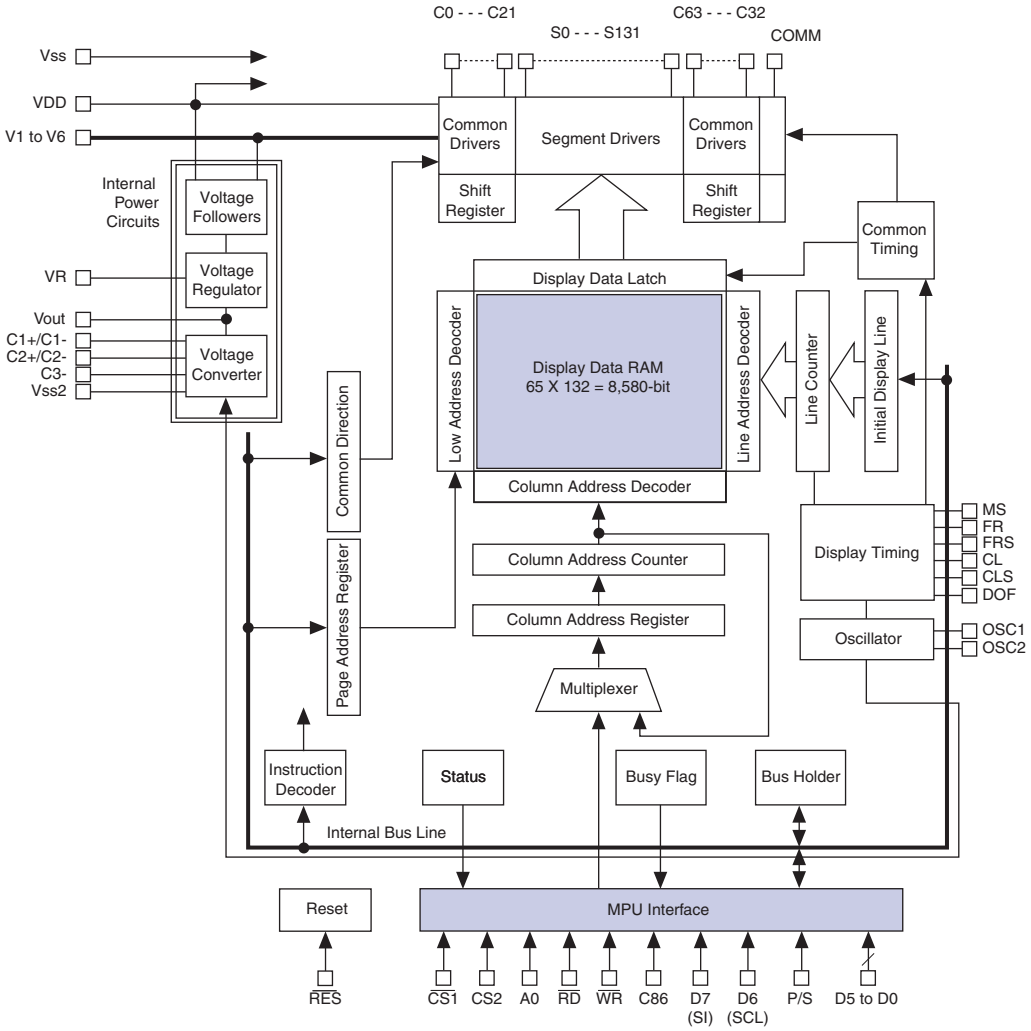
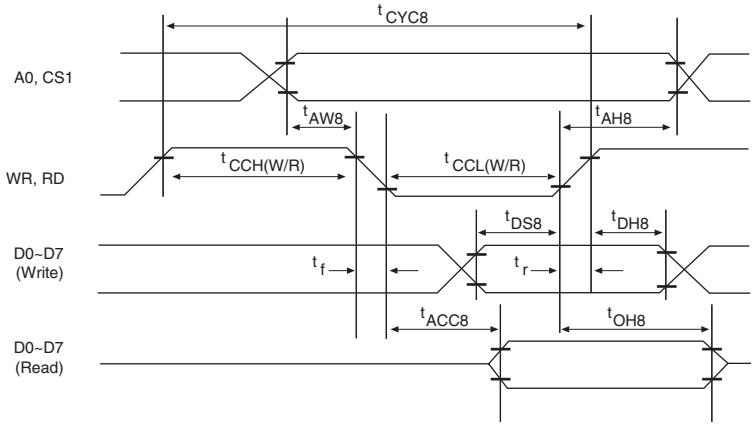


Figure 2–13 is an excerpt from the Optrex data sheet and shows the module interface signals for both read and write transactions.

**Figure 2–13. Graphics LCD Timing Diagram**




For more information about timing parameters, visit www.optrex.com.

Table 2–36 lists the graphics LCD display component reference and manufacturing information.

**Table 2–36. Graphics LCD Display Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| J24 | FPC/FFC 30-position flick lock connector, bottom contact | Hirose Electronics, Co. | FH12S-30S-0.55H(55) | www.hirose.com |
| | 128 × 64 graphics module, blue LCD (1) | Optrex America, Inc. | F-51852GNFQJ-LB-AIN | www.optrex.com |
| | 128 × 64 graphics module, green LCD (1) | Optrex America, Inc. | F-51852GNFQJ-LG-ACN | www.optrex.com |

**Note to Table 2–36:**

(1) The Stratix III development board is shipped with either a blue or green Optrex LCD display.

## Speaker Header

A four-pin 0.1 in. pitch header, board reference J1, is used for a PC speaker connection. The FPGA drives an R/C filter from a 2.5-V CMOS I/O pin allowing tones to be generated by driving different frequencies to the pin. Stratix III device pin AJ11 drives the input of the R/C filter (U1).

Table 2–37 lists speaker header component reference and manufacturing information.

**Table 2–37. Speaker Header Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| J1 | Speaker header | Samtec | TSW-104-07-G-S | www.samtec.com |

# Components and Interfaces

This section describes the board's communication ports and interface cards relative to the Stratix III device. The board supports the following communication ports:



## USB 2.0 MAC/PHY

The board incorporates the FTDI USB 2.0 PHY chip. The device interfaces to J5, a Type B USB connector. The maximum speed of the interface is 12 Mbps. Typical application speeds are around 1.5 Mbps; however, actual system speed may vary.

The primary usage for the USB device is to provide JTAG programming of on-board devices such as the FPGA and flash memory. The interface is also the default connection between the FPGA and the host PC applications such as SignalTap® II, DSP Builder, and the Nios© II JTAG universal asynchronous receiver/transmitter (UART).

For more information about the data sheet and related documentation, contact FTDI at www.ftdichip.com.

Table 2–38 lists the FTDI USB interface component reference and manufacturing information.

**Table 2–38. FTDI Interface Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U11 | FTDI USB device | FTDI Ltd. | FT245BL | www.ftdichip.com |

## 10/100/1000 Ethernet

A Marvell 88E1111 device is used for 10/100/1000 base-T Ethernet connection. The device is an auto-negotiating Ethernet PHY with a GMII, RGMII, or SGMII interface to the FPGA. Stratix III devices can communicate with LVDS interfaces at up to 1.25 Gbps, which is well above the 1.0 Gbps SGMII requirement. The MAC function must be provided in the FPGA for typical networking applications. The Marvell PHY uses 2.5-V and 1.1-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. It interfaces to a HALO HFJ11-1G02E model RJ-45 with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 2–14 and Figure 2–15 show the GMII and the SGMII interfaces between the FPGA (MAC) and Marvell PHY 88E1111 device.

**Figure 2–14. Marvell 88E1111 GMII Interface**

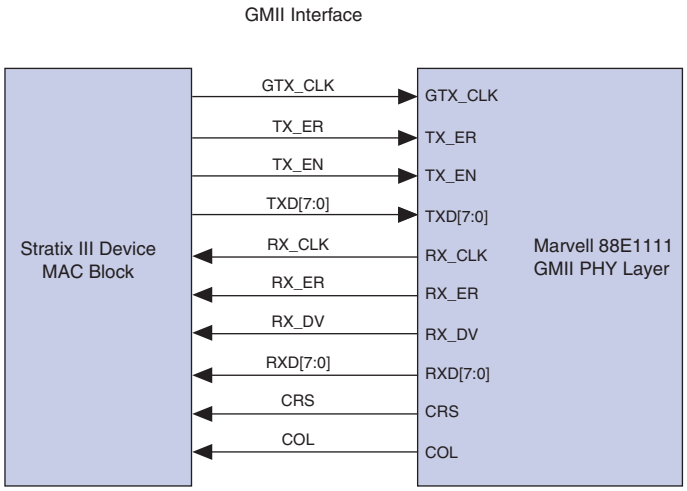



**Figure 2–15. Marvell 88E1111 SGMII Interface**

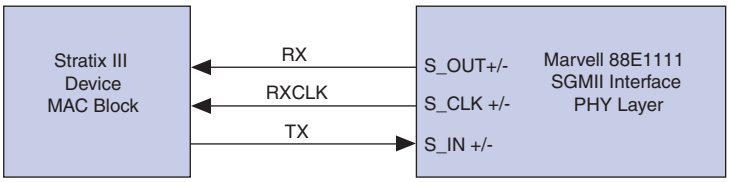



Table 2–39 lists the pins of the Gigabit Ethernet interface.

**Table 2–39. Ethernet PHY (U25) Pin-Out (Part 1 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| U25 pin 8 | RGMII interface transmit clock | ENET_GTX_CLK | 2.5 V | AB33 |
| U25 pin 23 | Management bus interrupt | ENET_INTn | 2.5 V | AB32 |
| U25 pin 73 | 1000 MBytes link established | ENET_LED_LINK1000 | 2.5 V | A28 |
| U25 pin 25 | Management bus data clock | ENET_MDC | 2.5 V | Y2 |
| U25 pin 24 | Management bus data | ENET_MDIO | 2.5 V | AD30 |
| U25 pin 28 | Reset | ENET_RESETN | 2.5 V | Y31 |
| U25 pin 2 | RGMII interface receive clock | ENET_RX_CLK | 1.8 V | AK28 |
| U25 pin 83 | GMII interface collision | ENET_RX_COL | 2.5 V | V33 |
| U25 pin 84 | GMII interface carrier sense | ENET_RX_CRS | 2.5 V | V3 |
| U25 pin 95 | GMII/ RGMII interface receive data bus bit 0 | ENET_RX_D0 | 2.5 V | AE29 |
| U25 pin 92 | GMII/ RGMII interface receive data bus bit 1 | ENET_RX_D1 | 2.5 V | AM34 |
| U25 pin 93 | GMII/ RGMII interface receive data bus bit 2 | ENET_RX_D2 | 2.5 V | AL33 |
| U25 pin 91 | GMII/ RGMII interface receive data bus bit 3 | ENET_RX_D3 | 2.5 V | AJ32 |

**Table 2–39. Ethernet PHY (U25) Pin-Out (Part 2 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| U25 pin 90 | GMII interface receive data bus bit 4 | ENET_RX_D4 | 2.5 V | AH34 |
| U25 pin 89 | GMII interface receive data bus bit 5 | ENET_RX_D5 | 2.5 V | AF29 |
| U25 pin 87 | GMII interface receive data bus bit 6 | ENET_RX_D6 | 2.5 V | AH33 |
| U25 pin 86 | GMII interface receive data bus bit 7 | ENET_RX_D7 | 2.5 V | V34 |
| U25 pin 94 | RGMII interface receive control | ENET_RX_DV | 2.5 V | W5 |
| U25 pin 3 | GMII interface receive error | ENET_RX_ER | 2.5 V | AJ10 |
| U25 pin 75 | SGMII interface receive data | ENET_RX_N | LVDS | Y34 |
| U25 pin 77 | SGMII interface receive data | ENET_RX_P | LVDS | AA33 |
| U25 pin 80 | SGMII interface (625 MHz) clock | ENET_S_CLKN | LVDS | W34 |
| U25 pin 79 | SGMII interface (625 MHz) clock | ENET_S_CLKP | LVDS | W33 |
| U25 pin 4 | MII interface (25 MHz) clock | ENET_TX_CLK | 2.5 V | AB34 |
| U25 pin 11 | RGMII interface transmit data bus bit 0 | ENET_TX_D[0] | 2.5 V | AF28 |
| U25 pin 12 | RGMII interface transmit data bus bit 1 | ENET_TX_D[1] | 2.5 V | AD34 |
| U25 pin 14 | RGMII interface transmit data bus bit 2 | ENET_TX_D[2] | 2.5 V | AL34 |
| U25 pin 16 | RGMII interface transmit data bus bit 3 | ENET_TX_D[3] | 2.5 V | W30 |
| U25 pin 17 | RGMII interface transmit data bus bit 4 | ENET_TX_D[4] | 2.5 V | AD33 |
| U25 pin 18 | RGMII interface transmit data bus bit 5 | ENET_TX_D[5] | 2.5 V | AJ34 |
| U25 pin 19 | RGMII interface transmit data bus bit 6 | ENET_TX_D[6] | 2.5 V | AJ31 |
| U25 pin 20 | RGMII interface transmit data bus bit 7 | ENET_TX_D[7] | 2.5 V | AG30 |
| U25 pin 9 | RGMII interface transmit control | ENET_TX_EN | 2.5 V | AA34 |
| U25 pin 7 | RGMII interface transmit error | ENET_TX_ER | 2.5 V | AA29 |
| U25 pin 81 | SGMII interface transmit data | ENET_TX_N | LVDS | V29 |
| U25 pin 82 | SGMII interface transmit data | ENET_TX_P | LVDS | W28 |

Table 2–40 lists the Ethernet PHY component reference and manufacturing information.

**Table 2–40. Ethernet PHY Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U25 | Ethernet PHY base-T device | Marvel Semiconductor | 88E1111-B2-CAAIC000 | www.marvell.com |

## High-Speed Mezzanine Cards

The board contains two HSMC interfaces called Port A and Port B. These HSMC interfaces support both single-ended and differential signaling. The connector part number is Samtec ASP-122953-01. The HSMC interface also allows for JTAG, SMBus, clock outputs and inputs, as well as power for compatible HSMCs.

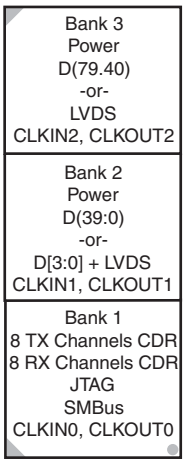
The HSMC is an Altera-developed specification, which allows users to expand the functionality of the development board through the addition of daughter cards (HSMCs).

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, visit www.altera.com.

The HSMC connector has 172 total pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting as both shield and reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as it is done in the QSH-DP/QTH-DP series. Banks 2 and 3 have all of the pins populated as it is done in the QSH/QTH series.

The Stratix III development board does not use bank 1 transceiver signals intended for clock-data-recover (CDR) applications such as PCI Express and Rapid I/O©. These 32 pins are left floating. Banks 2 and 3 are fully supported and can be used in two different configurations, as shown in Figure 2–16.

**Figure 2–16. HSMC Signal and Bank Diagram**




The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to LVDS, mini-LVDS, and RSDS with up to 17-channels full-duplex.

As noted in the HSMC specification, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or the generic differential pin-out.

For the Stratix III FPGA Development Kit, there is only one clock per HSMC interface that can drive a PLL. If you want to drive a PLL from the HSMC interface make sure you use either `HSMA_CLK_P2` for Port A or `HSMB_CLK_P2` for Port B.

*Section 2.2.4* of the *HSMC Specification* recommends that a dedicated clock input be used for the single-ended clock (CMOS CLK) on pin 40 of the HSMC connector. The Stratix III board uses a regular input pin due to lack of input clock resources. This means that clocks driven from the HSMC cannot be routed to a PLL. This limitation is true for both HSMC Port A and HSMC Port B.

*Section 2.2.5* of the *HSMC Specification* recommends that dedicated clock inputs are used for the differential LVDS clocks (LVDS CLK/CMOS) on pin pairs (96, 98) and (156, 158) of the HSMC connector. The specification makes `CLKIN2p/n` the priority as such the Stratix III board has a standard LVDS input pair due to lack of input clock resources. This means that the clock driven into `CLKIN1p/n` from the HSMC cannot be routed to a PLL. This limitation is true for both HSMC Port A and HSMC Port B.

If you must use another clock, you can drive the clock to the SMA output of the board, then attach a cable from the SMA output to the SMA input. In this case, assign the Stratix III pin that corresponds to the SMA input as your clock.

Table 2–41 lists the HSMC Port A interface signal name, description, and signal type.

**Table 2–41. HSMC Port A Interface Signal Name, Description, and Type (Part 1 of 3)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J18 pin 33 | Management serial data | HSMA_SDA | 2.5 V | P8 |
| J18 pin 34 | Management serial clock | HSMA_SCL | 2.5 V | AA32 |
| J18 pin 35 | JTAG clock signal | FPGA_JTAG_TCK | 2.5 V | F30 |
| J18 pin 36 | JTAG mode select signal | FPGA_JTAG_TMS | 2.5 V | N/A |
| J18 pin 37 | JTAG data output | HSMA_JTAG_TDO | 2.5 V | N/A |
| J18 pin 38 | JTAG data input | HSMA_JTAG_TDI | 2.5 V | N/A |
| J18 pin 39 | Dedicated CMOS clock out | HSMA_CLK_OUT0 | 2.5 V | AD28 |
| J18 pin 40 | Dedicated CMOS clock in | HSMA_CLK_IN0 | 2.5 V | W10 |
| J18 pin 41 | Dedicated CMOS I/O bit 0 | HSMA_D0 | 2.5 V | AK9 |
| J18 pin 42 | Dedicated CMOS I/O bit 1 | HSMA_D1 | 2.5 V | AJ9 |
| J18 pin 43 | Dedicated CMOS I/O bit 2 | HSMA_D2 | 2.5 V | AL7 |
| J18 pin 44 | Dedicated CMOS I/O bit 3 | HSMA_D3 | 2.5 V | AL9 |
| J18 pin 47 | LVDS TX or CMOS I/O bit 0 | HSMA_TX_P0 | LVDS or 2.5 V | AC11 |
| J18 pin 48 | LVDS RX or CMOS I/O bit 0 | HSMA_RX_P0 | LVDS or 2.5 V | AJ4 |
| J18 pin 49 | LVDS TX or CMOS I/O bit 0 | HSMA_TX_N0 | LVDS or 2.5 V | AB10 |
| J18 pin 50 | LVDS RX or CMOS I/O bit 0 | HSMA_RX_N0 | LVDS or 2.5 V | AJ3 |
| J18 pin 53 | LVDS TX or CMOS I/O bit 1 | HSMA_TX_P1 | LVDS or 2.5 V | AC9 |
| J18 pin 54 | LVDS RX or CMOS I/O bit 1 | HSMA_RX_P1 | LVDS or 2.5 V | AG4 |
| J18 pin 55 | LVDS TX or CMOS I/O bit 1 | HSMA_TX_N1 | LVDS or 2.5 V | AC8 |
| J18 pin 56 | LVDS RX or CMOS I/O bit 1 | HSMA_RX_N1 | LVDS or 2.5 V | AG3 |
| J18 pin 59 | LVDS TX or CMOS I/O bit 2 | HSMA_TX_P2 | LVDS or 2.5 V | AH5 |
| J18 pin 60 | LVDS RX or CMOS I/O bit 2 | HSMA_RX_P2 | LVDS or 2.5 V | AM2 |
| J18 pin 61 | LVDS TX or CMOS I/O bit 2 | HSMA_TX_N2 | LVDS or 2.5 V | AH4 |
| J18 pin 62 | LVDS RX or CMOS I/O bit 2 | HSMA_RX_N2 | LVDS or 2.5 V | AM1 |
| J18 pin 65 | LVDS TX or CMOS I/O bit 3 | HSMA_TX_P3 | LVDS or 2.5 V | AE8 |
| J18 pin 66 | LVDS RX or CMOS I/O bit 3 | HSMA_RX_P3 | LVDS or 2.5 V | AL2 |
| J18 pin 67 | LVDS TX or CMOS I/O bit 3 | HSMA_TX_N3 | LVDS or 2.5 V | AE7 |
| J18 pin 68 | LVDS RX or CMOS I/O bit 3 | HSMA_RX_N3 | LVDS or 2.5 V | AL1 |
| J18 pin 71 | LVDS TX or CMOS I/O bit 4 | HSMA_TX_P4 | LVDS or 2.5 V | AF6 |

**Table 2–41. HSMC Port A Interface Signal Name, Description, and Type (Part 2 of 3)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J18 pin 72 | LVDS RX or CMOS I/O bit 4 | HSMA_RX_P4 | LVDS or 2.V5 | AJ2 |
| J18 pin 73 | LVDS TX or CMOS I/O bit 4 | HSMA_TX_N4 | LVDS or 2.5 V | AF5 |
| J18 pin 74 | LVDS RX or CMOS I/O bit 4 | HSMA_RX_N4 | LVDS or 2.5 V | AK1 |
| J18 pin 77 | LVDS TX or CMOS I/O bit 5 | HSMA_TX_P5 | LVDS or 2.5 V | AD7 |
| J18 pin 78 | LVDS RX or CMOS I/O bit 5 | HSMA_RX_P5 | LVDS or 2.5 V | AH2 |
| J18 pin 79 | LVDS TX or CMOS I/O bit 5 | HSMA_TX_N5 | LVDS or 2.5 V | AD6 |
| J18 pin 80 | LVDS RX or CMOS I/O bit 5 | HSMA_RX_N5 | LVDS or 2.5 V | AJ1 |
| J18 pin 83 | LVDS TX or CMOS I/O bit 6 | HSMA_TX_P6 | LVDS or 2.5 V | AE6 |
| J18 pin 84 | LVDS RX or CMOS I/O bit 6 | HSMA_RX_P6 | LVDS or 2.5 V | AF4 |
| J18 pin 85 | LVDS TX or CMOS I/O bit 6 | HSMA_TX_N6 | LVDS or 2.5 V | AE5 |
| J18 pin 86 | LVDS RX or CMOS I/O bit 6 | HSMA_RX_N6 | LVDS or 2.5 V | AF3 |
| J18 pin 89 | LVDS TX or CMOS I/O bit 7 | HSMA_TX_P7 | LVDS or 2.5 V | AD4 |
| J18 pin 90 | LVDS RX or CMOS I/O bit 7 | HSMA_RX_P7 | LVDS or 2.5 V | AG1 |
| J18 pin 91 | LVDS TX or CMOS I/O bit 7 | HSMA_TX_N7 | LVDS or 2.5 V | AD3 |
| J18 pin 92 | LVDS RX or CMOS I/O bit 7 | HSMA_RX_N7 | LVDS or 2.5 V | AH1 |
| J18 pin 95 | LVDS or CMOS clock out | HSMA_CLK_OUT_P1 | LVDS or 2.5 V | V10 |
| J18 pin 96 | LVDS or CMOS clock in | HSMA_CLK_IN_P1 | LVDS or 2.5 V | Y4 |
| J18 pin 97 | LVDS or CMOS clock out | HSMA_CLK_OUT_N1 | LVDS or 2.5 V | W9 |
| J18 pin 98 | LVDS or CMOS clock in | HSMA_CLK_IN_N1 | LVDS or 2.5 V | W3 |
| J18 pin 101 | LVDS TX or CMOS I/O bit 8 | HSMA_TX_P8 | LVDS or 2.5 V | AC6 |
| J18 pin 102 | LVDS RX or CMOS I/O bit 8 | HSMA_RX_P8 | LVDS or 2.5 V | AF2 |
| J18 pin 103 | LVDS TX or CMOS I/O bit 8 | HSMA_TX_N8 | LVDS or 2.5 V | AC5 |
| J18 pin 104 | LVDS RX or CMOS I/O bit 8 | HSMA_RX_N8 | LVDS or 2.5 V | AF1 |
| J18 pin 107 | LVDS TX or CMOS I/O bit 9 | HSMA_TX_P9 | LVDS or 2.5 V | AB6 |
| J18 pin 108 | LVDS RX or CMOS I/O bit 9 | HSMA_RX_P9 | LVDS or 2.5 V | AE2 |
| J18 pin 109 | LVDS TX or CMOS I/O bit 9 | HSMA_TX_N9 | LVDS or 2.5 V | AB5 |
| J18 pin 110 | LVDS RX or CMOS I/O bit 9 | HSMA_RX_N9 | LVDS or 2.5 V | AE1 |
| J18 pin 113 | LVDS TX or CMOS I/O bit 10 | HSMA_TX_P10 | LVDS or 2.5 V | AB8 |
| J18 pin 114 | LVDS RX or CMOS I/O bit 10 | HSMA_RX_P10 | LVDS or 2.5 V | AE4 |
| J18 pin 115 | LVDS TX or CMOS I/O bit 10 | HSMA_TX_N10 | LVDS or 2.5 V | AC7 |
| J18 pin 116 | LVDS RX or CMOS I/O bit 10 | HSMA_RX_N10 | LVDS or 2.5 V | AE3 |
| J18 pin 119 | LVDS TX or CMOS I/O bit 11 | HSMA_TX_P11 | LVDS or 2.5 V | Y6 |
| J18 pin 120 | LVDS RX or CMOS I/O bit 11 | HSMA_RX_P11 | LVDS or 2.5 V | AC2 |
| J18 pin 121 | LVDS TX or CMOS I/O bit 11 | HSMA_TX_N11 | LVDS or 2.5 V | Y5 |
| J18 pin 122 | LVDS RX or CMOS I/O bit 11 | HSMA_RX_N11 | LVDS or 2.5 V | AD1 |
| J18 pin 125 | LVDS TX or CMOS I/O bit 12 | HSMA_TX_P12 | LVDS or 2.5 V | AA7 |
| J18 pin 126 | LVDS RX or CMOS I/O bit 12 | HSMA_RX_P12 | LVDS or 2.5 V | AB2 |
| J18 pin 127 | LVDS TX or CMOS I/O bit 12 | HSMA_TX_N12 | LVDS or 2.5 V | AA6 |
| J18 pin 128 | LVDS RX or CMOS I/O bit 12 | HSMA_RX_N12 | LVDS or 2.5 V | AC1 |

**Table 2–41. HSMC Port A Interface Signal Name, Description, and Type (Part 3 of 3)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J18 pin 131 | LVDS TX or CMOS I/O bit 13 | HSMA_TX_P13 | LVDS or 2.5 V | Y8 |
| J18 pin 132 | LVDS RX or CMOS I/O bit 13 | HSMA_RX_P13 | LVDS or 2.5 V | AA1 |
| J18 pin 133 | LVDS TX or CMOS I/O bit 13 | HSMA_TX_N13 | LVDS or 2.5 V | Y7 |
| J18 pin 134 | LVDS RX or CMOS I/O bit 13 | HSMA_RX_N13 | LVDS or 2.5 V | AB1 |
| J18 pin 137 | LVDS TX or CMOS I/O bit 14 | HSMA_TX_P14 | LVDS or 2.5 V | Y10 |
| J18 pin 138 | LVDS RX or CMOS I/O bit 14 | HSMA_RX_P14 | LVDS or 2.5 V | AC4 |
| J18 pin 139 | LVDS TX or CMOS I/O bit 14 | HSMA_TX_N14 | LVDS or 2.5 V | Y9 |
| J18 pin 140 | LVDS RX or CMOS I/O bit 14 | HSMA_RX_N14 | LVDS or 2.5 V | AB3 |
| J18 pin 143 | LVDS TX or CMOS I/O bit 15 | HSMA_TX_P15 | LVDS or 2.5 V | W12 |
| J18 pin 144 | LVDS RX or CMOS I/O bit 15 | HSMA_RX_P15 | LVDS or 2.5 V | AB4 |
| J18 pin 145 | LVDS TX or CMOS I/O bit 15 | HSMA_TX_N15 | LVDS or 2.5 V | Y11 |
| J18 pin 146 | LVDS RX or CMOS I/O bit 15 | HSMA_RX_N15 | LVDS or 2.5 V | AA3 |
| J18 pin 149 | LVDS TX or CMOS I/O bit 16 | HSMA_TX_P16 | LVDS or 2.5 V | AA12 |
| J18 pin 150 | LVDS RX or CMOS I/O bit 16 | HSMA_RX_P16 | LVDS or 2.5 V | AA4 |
| J18 pin 151 | LVDS TX or CMOS I/O bit 16 | HSMA_TX_N16 | LVDS or 2.5 V | AB11 |
| J18 pin 152 | LVDS RX or CMOS I/O bit 16 | HSMA_RX_N16 | LVDS or 2.5 V | Y3 |
| J18 pin 155 | LVDS or CMOS clock out | HSMA_CLK_OUT_P2 | LVDS | W8 |
| J18 pin 156 | LVDS or CMOS clock in | HSMA_CLK_IN_P2 | LVDS | T2 |
| J18 pin 157 | LVDS or CMOS clock out | HSMA_CLK_OUT_N2 | 2.5 V | W7 |
| J18 pin 158 | LVDS or CMOS clock in | HSMA_CLK_IN_N2 | 2.5 V | T1 |
| N/A | User LED intended to show RX data activity on the HSMC interface | HSMA_RX_LED | 2.5 V | Y25 |
| N/A | User LED intended to show TX data activity on the HSMC interface | HSMA_TX_LED | 2.5 V | AG29 |

Table 2–42 lists the HSMC Port B interface signal name, description, and signal type.

**Table 2–42. HSMC Port B Interface Signal Name, Description, and Type (Part 1 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J8 pin 33 | Serial data | HSMB_SDA | 2.5 V | U11 |
| J8 pin 34 | Serial clock | HSMB_SCL | 2.5 V | AD31 |
| J8 pin 35 | JTAG clock signal | FPGA_JTAG_TCK | 2.5 V | F30 |
| J8 pin 36 | JTAG mode select signal | FPGA_JTAG_TMS | 2.5 V | N/A |
| J8 pin 37 | JTAG data output | HSMB_JTAG_TDO | 2.5 V | G28 |
| J8 pin 38 | JTAG data input | HSMB_JTAG_TDI | 2.5 V | N/A |
| J8 pin 39 | Dedicated CMOS clock out | HSMB_CLK_OUT0 | 2.5 V | AC34 |
| J8 pin 40 | Dedicated CMOS clock in | HSMB_CLK_IN0 | 2.5 V | V4 |
| J8 pin 41 | Dedicated CMOS I/O bit 0 | HSMB_D0 | 2.5 V | AB24 |
| J8 pin 42 | Dedicated CMOS I/O bit 1 | HSMB_D1 | 2.5 V | AB25 |

**Table 2–42. HSMC Port B Interface Signal Name, Description, and Type (Part 2 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J8 pin 43 | Dedicated CMOS I/O bit 2 | HSMB_D2 | 2.5 V | AF32 |
| J8 pin 44 | Dedicated CMOS I/O bit 3 | HSMB_D3 | 2.5 V | AF31 |
| J8 pin 47 | LVDS TX or CMOS I/O bit 0 | HSMB_TX_P0 | LVDS or 2.5 V | P11 |
| J8 pin 48 | LVDS RX or CMOS I/O bit 0 | HSMB_RX_P0 | LVDS or 2.5 V | R4 |
| J8 pin 49 | LVDS TX or CMOS I/O bit 0 | HSMB_TX_N0 | LVDS or 2.5 V | P10 |
| J8 pin 50 | LVDS RX or CMOS I/O bit 0 | HSMB_RX_N0 | LVDS or 2.5 V | R3 |
| J8 pin 53 | LVDS TX or CMOS I/O bit 1 | HSMB_TX_P1 | LVDS or 2.5 V | T9 |
| J8 pin 54 | LVDS RX or CMOS I/O bit 1 | HSMB_RX_P1 | LVDS or 2.5 V | P4 |
| J8 pin 55 | LVDS TX or CMOS I/O bit 1 | HSMB_TX_N1 | LVDS or 2.5 V | T8 |
| J8 pin 56 | LVDS RX or CMOS I/O bit 1 | HSMB_RX_N1 | LVDS or 2.5 V | P3 |
| J8 pin 59 | LVDS TX or CMOS I/O bit 2 | HSMB_TX_P2 | LVDS or 2.5 V | T7 |
| J8 pin 60 | LVDS RX or CMOS I/O bit 2 | HSMB_RX_P2 | LVDS or 2.5 V | P2 |
| J8 pin 61 | LVDS TX or CMOS I/O bit 2 | HSMB_TX_N2 | LVDS or 2.5 V | U6 |
| J8 pin 62 | LVDS RX or CMOS I/O bit 2 | HSMB_RX_N2 | LVDS or 2.5 V | R1 |
| J8 pin 65 | LVDS TX or CMOS I/O bit 3 | HSMB_TX_P3 | LVDS or 2.5 V | T5 |
| J8 pin 66 | LVDS RX or CMOS I/O bit 3 | HSMB_RX_P3 | LVDS or 2.5 V | N2 |
| J8 pin 67 | LVDS TX or CMOS I/O bit 3 | HSMB_TX_N3 | LVDS or 2.5 V | T4 |
| J8 pin 68 | LVDS RX or CMOS I/O bit 3 | HSMB_RX_N3 | LVDS or 2.5 V | P1 |
| J8 pin 71 | LVDS TX or CMOS I/O bit 4 | HSMB_TX_P4 | LVDS or 2.5 V | R10 |
| J8 pin 72 | LVDS RX or CMOS I/O bit 4 | HSMB_RX_P4 | LVDS or 2.5 V | M1 |
| J8 pin 73 | LVDS TX or CMOS I/O bit 4 | HSMB_TX_N4 | LVDS or 2.5 V | R9 |
| J8 pin 74 | LVDS RX or CMOS I/O bit 4 | HSMB_RX_N4 | LVDS or 2.5 V | N1 |
| J8 pin 77 | LVDS TX or CMOS I/O bit 5 | HSMB_TX_P5 | LVDS or 2.5 V | R7 |
| J8 pin 78 | LVDS RX or CMOS I/O bit 5 | HSMB_RX_P5 | LVDS or 2.5 V | L2 |
| J8 pin 79 | LVDS TX or CMOS I/O bit 5 | HSMB_TX_N5 | LVDS or 2.5 V | R6 |
| J8 pin 80 | LVDS RX or CMOS I/O bit 5 | HSMB_RX_N5 | LVDS or 2.5 V | L1 |
| J8 pin 83 | LVDS TX or CMOS I/O bit 6 | HSMB_TX_P6 | LVDS or 2.5 V | N9 |
| J8 pin 84 | LVDS RX or CMOS I/O bit 6 | HSMB_RX_P6 | LVDS or 2.5 V | K4 |
| J8 pin 85 | LVDS TX or CMOS I/O bit 6 | HSMB_TX_N6 | LVDS or 2.5 V | N8 |
| J8 pin 86 | LVDS RX or CMOS I/O bit 6 | HSMB_RX_N6 | LVDS or 2.5 V | K3 |
| J8 pin 89 | LVDS TX or CMOS I/O bit 7 | HSMB_TX_P7 | LVDS or 2.5 V | M7 |
| J8 pin 90 | LVDS RX or CMOS I/O bit 7 | HSMB_RX_P7 | LVDS or 2.5 V | J4 |
| J8 pin 91 | LVDS TX or CMOS I/O bit 7 | HSMB_TX_N7 | LVDS or 2.5 V | M6 |
| J8 pin 92 | LVDS RX or CMOS I/O bit 7 | HSMB_RX_N7 | LVDS or 2.5 V | J3 |
| J8 pin 95 | LVDS or CMOS clock out | HSMB_CLK_OUT_P1 | LVDS or 2.5 V | P6 |
| J8 pin 96 | LVDS or CMOS clock in | HSMB_CLK_IN_P1 | LVDS or 2.5 V | N4 |
| J8 pin 97 | LVDS or CMOS clock out | HSMB_CLK_OUT_N1 | LVDS or 2.5 V | P5 |
| J8 pin 98 | LVDS or CMOS clock in | HSMB_CLK_IN_N1 | LVDS or 2.5 V | N3 |
| J8 pin 101 | LVDS TX or CMOS I/O bit 8 | HSMB_TX_P8 | LVDS or 2.5 V | L7 |

**Table 2–42. HSMC Port B Interface Signal Name, Description, and Type (Part 3 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J8 pin 102 | LVDS RX or CMOS I/O bit 8 | HSMB_RX_P8 | LVDS or 2.5 V | H2 |
| J8 pin 103 | LVDS TX or CMOS I/O bit 8 | HSMB_TX_N8 | LVDS or 2.5 V | L6 |
| J8 pin 104 | LVDS RX or CMOS I/O bit 8 | HSMB_RX_N8 | LVDS or 2.5 V | J1 |
| J8 pin 107 | LVDS TX or CMOS I/O bit 9 | HSMB_TX_P9 | LVDS or 2.5 V | L5 |
| J8 pin 108 | LVDS TX or CMOS I/O bit 9 | HSMB_RX_P9 | LVDS or 2.5 V | G2 |
| J8 pin 109 | LVDS RX or CMOS I/O bit 9 | HSMB_TX_N9 | LVDS or 2.5 V | L4 |
| J8 pin 110 | LVDS RX or CMOS I/O bit 9 | HSMB_RX_N9 | LVDS or 2.5 V | H1 |
| J8 pin 113 | LVDS TX or CMOS I/O bit 10 | HSMB_TX_P10 | LVDS or 2.5 V | K6 |
| J8 pin 114 | LVDS RX or CMOS I/O bit 10 | HSMB_RX_P10 | LVDS or 2.5 V | F1 |
| J8 pin 115 | LVDS TX or CMOS I/O bit 10 | HSMB_TX_N10 | LVDS or 2.5 V | K5 |
| J8 pin 116 | LVDS RX or CMOS I/O bit 10 | HSMB_RX_N10 | LVDS or 2.5 V | G1 |
| J8 pin 119 | LVDS TX or CMOS I/O bit 11 | HSMB_TX_P11 | LVDS or 2.5 V | J7 |
| J8 pin 120 | LVDS RX or CMOS I/O bit 11 | HSMB_RX_P11 | LVDS or 2.5 V | H4 |
| J8 pin 121 | LVDS TX or CMOS I/O bit 11 | HSMB_TX_N11 | LVDS or 2.5 V | J6 |
| J8 pin 122 | LVDS RX or CMOS I/O bit 11 | HSMB_RX_N11 | LVDS or 2.5 V | H3 |
| J8 pin 125 | LVDS TX or CMOS I/O bit 12 | HSMB_TX_P12 | LVDS or 2.5 V | H6 |
| J8 pin 126 | LVDS RX or CMOS I/O bit 12 | HSMB_RX_P12 | LVDS or 2.5 V | E2 |
| J8 pin 127 | LVDS TX or CMOS I/O bit 12 | HSMB_TX_N12 | LVDS or 2.5 V | H5 |
| J8 pin 128 | LVDS RX or CMOS I/O bit 12 | HSMB_RX_N12 | LVDS or 2.5 V | E1 |
| J8 pin 131 | LVDS TX or CMOS I/O bit 13 | HSMB_TX_P13 | LVDS or 2.5 V | K8 |
| J8 pin 132 | LVDS RX or CMOS I/O bit 13 | HSMB_RX_P13 | LVDS or 2.5 V | C1 |
| J8 pin 133 | LVDS TX or CMOS I/O bit 13 | HSMB_TX_N13 | LVDS or 2.5 V | K7 |
| J8 pin 134 | LVDS RX or CMOS I/O bit 13 | HSMB_RX_N13 | LVDS or 2.5 V | D1 |
| J8 pin 137 | LVDS TX or CMOS I/O bit 14 | HSMB_TX_P14 | LVDS or 2.5 V | L8 |
| J8 pin 138 | LVDS RX or CMOS I/O bit 14 | HSMB_RX_P14 | LVDS or 2.5 V | D3 |
| J8 pin 139 | LVDS TX or CMOS I/O bit 14 | HSMB_TX_N14 | LVDS or 2.5 V | L8 |
| J8 pin 140 | LVDS RX or CMOS I/O bit 14 | HSMB_RX_N14 | LVDS or 2.5 V | D2 |
| J8 pin 143 | LVDS TX or CMOS I/O bit 15 | HSMB_TX_P15 | LVDS or 2.5 V | M10 |
| J8 pin 144 | LVDS RX or CMOS I/O bit 15 | HSMB_RX_P15 | LVDS or 2.5 V | G5 |
| J8 pin 145 | LVDS TX or CMOS I/O bit 15 | HSMB_TX_N15 | LVDS or 2.5 V | M9 |
| J8 pin 146 | LVDS RX or CMOS I/O bit 15 | HSMB_RX_N15 | LVDS or 2.5 V | G4 |
| J8 pin 149 | LVDS TX or CMOS I/O bit 16 | HSMB_TX_P16 | LVDS or 2.5 V | N11 |
| J8 pin 150 | LVDS RX or CMOS I/O bit 16 | HSMB_RX_P16 | LVDS or 2.5 V | F4 |
| J8 pin 151 | LVDS TX or CMOS I/O bit 16 | HSMB_TX_N16 | LVDS or 2.5 V | N10 |
| J8 pin 152 | LVDS RX or CMOS I/O bit 16 | HSMB_RX_N16 | LVDS or 2.5 V | F3 |
| J8 pin 155 | LVDS or CMOS clock out | HSMB_CLK_OUT_P2 | LVDS | R12 |
| J8 pin 156 | LVDS or CMOS clock in | HSMB_CLK_IN_P2 | LVDS | U4 |
| J8 pin 157 | LVDS or CMOS clock out | HSMB_CLK_OUT_N2 | 2.5 V | T11 |
| J8 pin 158 | LVDS or CMOS clock in | HSMB_CLK_IN_N2 | 2.5 V | U3 |

**Table 2–42. HSMC Port B Interface Signal Name, Description, and Type (Part 4 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| N/A | User LED intended to show RX Data activity on the HSMC | HSMB_RX_LED | 2.5 V | AJ12 |
| N/A | User LED intended to show TX Data activity on the HSMC | HSMB_TX_LED | 2.5 V | AG34 |

The board provides both 12-V and 3.3-V power supply to install daughter cards up to 18.6 W each. Table 2–43 shows the maximum current allowed per voltage.

**Table 2–43. HSMC Power Supply**

| Voltage | Minimum Current From Host | Minimum Wattage |
|---|---|---|
| 12 V | 1.0 A | 12.0 W |
| 3.3 V | 2.0 A | 6.6 W |

Table 2–44 lists HSMC component reference and manufacturing information.

**Table 2–44. HSMC Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| J8 and J18 | High-speed mezzanine card (HSMC), custom version of QSH-DP family high-speed socket | Samtec | ASP-122953-01 | www.samtec.com |

# On-Board Memory

This section describes the on-board memory interface support, and provides signal name, type, and signal connectivity relative to the Stratix III device.

The board has the following on-board memory:

- "DDR2 SDRAM DIMM" on page 2–49
- "DDR2 SDRAM Devices" on page 2–53
- "QDRII+ SRAM " on page 2–55
- "P-SRAM" on page 2–58
- "Flash Memory" on page 2–63

For more information, refer to:

- AN 435: Using DDR and DDR2 SDRAM in Stratix III and Stratix IV Devices
- AN 438: Constraining and Analyzing Timing for External Memory Interfaces in Stratix III and Cyclone III Devices

## DDR2 SDRAM DIMM

The board has 1 GByte DDR2 SDRAM DIMM memory interface with a 72-bit data width on the vertical I/O banks, which is typically used as a 64-bit interface with the additional 8 bits serving as error correction coding (ECC) bits for each of the 8-byte lanes. The target frequency is 400 MHz (800 Mbps) with potential operation of up to 533 MHz (1,066 Mbps). The theoretical bandwidth of the entire DDR2 interface is 6,388 Mbps plus ECC, or 7,187 Mbps raw throughput.

The data interface to the FPGA fabric runs at either one-half or one-quarter the physical layer data rate when using the Altera DDR2 MegaCore® function, which equates to a doubling or quadrupling of the physical data bus width (144 bits or 288 bits, respectively). For example, a 72-bit interface with a 400-MHz external clock speed can have a 400-MHz 144-bit internal bus or a 200-MHz 288-bit interface.

Table 2–45 lists the DDR2 DIMM interface signals. Signal names and type are relative to the Stratix III device regarding the I/O setting and direction. JEDEC bus widths are used.

**Table 2–45. DDR2 DIMM Interface I/O Signals (Part 1 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J19 pin 188 | Address bit 0 | DDR2_DIMM_A0 | SSTL-18 class I | AM19 |
| J19 pin 183 | Address bit 1 | DDR2_DIMM_A1 | SSTL-18 class I | AM18 |
| J19 pin 63 | Address bit 2 | DDR2_DIMM_A2 | SSTL-18 class I | AF16 |
| J19 pin 182 | Address bit 3 | DDR2_DIMM_A3 | SSTL-18 class I | AN16 |
| J19 pin 61 | Address bit 4 | DDR2_DIMM_A4 | SSTL-18 class I | AM17 |
| J19 pin 60 | Address bit 5 | DDR2_DIMM_A5 | SSTL-18 class I | AL19 |
| J19 pin 180 | Address bit 6 | DDR2_DIMM_A6 | SSTL-18 class I | AK18 |
| J19 pin 58 | Address bit 7 | DDR2_DIMM_A7 | SSTL-18 class I | AD16 |
| J19 pin 179 | Address bit 8 | DDR2_DIMM_A8 | SSTL-18 class I | AE16 |
| J19 pin 177 | Address bit 9 | DDR2_DIMM_A9 | SSTL-18 class I | AM16 |
| J19 pin 70 | Address bit 10 | DDR2_DIMM_A10 | SSTL-18 class I | AH19 |
| J19 pin 57 | Address bit 11 | DDR2_DIMM_A11 | SSTL-18 class I | AL16 |
| J19 pin 176 | Address bit 12 | DDR2_DIMM_A12 | SSTL-18 class I | AF20 |
| J19 pin 196 | Address bit 13 | DDR2_DIMM_A13 | SSTL-18 class I | AE23 |
| J19 pin 174 | Address bit 14 | DDR2_DIMM_A14 | SSTL-18 class I | AG19 |
| J19 pin 173 | Address bit 15 | DDR2_DIMM_A15 | SSTL-18 class I | AP12 |
| J19 pin 71 | Bank address bit 0 | DDR2_DIMM_BA0 | SSTL-18 class I | AN18 |
| J19 pin 190 | Bank address bit 1 | DDR2_DIMM_BA1 | SSTL-18 class I | AL17 |
| J19 pin 54 | Bank address bit 2 | DDR2_DIMM_BA2 | SSTL-18 class I | AD15 |
| J19 pin 125 | Data write mask (byte enables) bit 0 | DDR2_DIMM_DM0 | SSTL-18 class I | AL12 |
| J19 pin 134 | Data write mask (byte enables) bit 1 | DDR2_DIMM_DM1 | SSTL-18 class I | AP10 |
| J19 pin 146 | Data write mask (byte enables) bit 2 | DDR2_DIMM_DM2 | SSTL-18 class I | AJ15 |
| J19 pin 155 | Data write mask (byte enables) bit 3 | DDR2_DIMM_DM3 | SSTL-18 class I | AL22 |
| J19 pin 202 | Data write mask (byte enables) bit 4 | DDR2_DIMM_DM4 | SSTL-18 class I | AE22 |

**Table 2–45. DDR2 DIMM Interface I/O Signals (Part 2 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J19 pin 211 | Data write mask (byte enables) bit 5 | DDR2_DIMM_DM5 | SSTL-18 class I | AK27 |
| J19 pin 223 | Data write mask (byte enables) bit 6 | DDR2_DIMM_DM6 | SSTL-18 class I | AJ28 |
| J19 pin 232 | Data write mask (byte enables) bit 7 | DDR2_DIMM_DM7 | SSTL-18 class I | AP32 |
| J19 pin 164 | Data write mask (byte enables) bit 8 | DDR2_DIMM_DM8 | SSTL-18 class I | AH23 |
| J19 pin 3 | Data bit 0 | DDR2_DIMM_DQ0 | SSTL-18 class I | AP6 |
| J19 pin 4 | Data bit 1 | DDR2_DIMM_DQ1 | SSTL-18 class I | AN7 |
| J19 pin 9 | Data bit 2 | DDR2_DIMM_DQ2 | SSTL-18 class I | AK10 |
| J19 pin 10 | Data bit 3 | DDR2_DIMM_DQ3 | SSTL-18 class I | AK12 |
| J19 pin 122 | Data bit 4 | DDR2_DIMM_DQ4 | SSTL-18 class I | AM7 |
| J19 pin 123 | Data bit 5 | DDR2_DIMM_DQ5 | SSTL-18 class I | AM8 |
| J19 pin 128 | Data bit 6 | DDR2_DIMM_DQ6 | SSTL-18 class I | AM11 |
| J19 pin 129 | Data bit 7 | DDR2_DIMM_DQ7 | SSTL-18 class I | AP8 |
| J19 pin 12 | Data bit 8 | DDR2_DIMM_DQ8 | SSTL-18 class I | AE13 |
| J19 pin 13 | Data bit 9 | DDR2_DIMM_DQ9 | SSTL-18 class I | AF13 |
| J19 pin 21 | Data bit 10 | DDR2_DIMM_DQ10 | SSTL-18 class I | AP11 |
| J19 pin 22 | Data bit 11 | DDR2_DIMM_DQ11 | SSTL-18 class I | AF15 |
| J19 pin 131 | Data bit 12 | DDR2_DIMM_DQ12 | SSTL-18 class I | AE14 |
| J19 pin 132 | Data bit 13 | DDR2_DIMM_DQ13 | SSTL-18 class I | AE15 |
| J19 pin 140 | Data bit 14 | DDR2_DIMM_DQ14 | SSTL-18 class I | AP9 |
| J19 pin 141 | Data bit 15 | DDR2_DIMM_DQ15 | SSTL-18 class I | AN10 |
| J19 pin 24 | Data bit 16 | DDR2_DIMM_DQ16 | SSTL-18 class I | AN12 |
| J19 pin 25 | Data bit 17 | DDR2_DIMM_DQ17 | SSTL-18 class I | AM12 |
| J19 pin 30 | Data bit 18 | DDR2_DIMM_DQ18 | SSTL-18 class I | AG15 |
| J19 pin 31 | Data bit 19 | DDR2_DIMM_DQ19 | SSTL-18 class I | AH15 |
| J19 pin 143 | Data bit 20 | DDR2_DIMM_DQ20 | SSTL-18 class I | AN13 |
| J19 pin 144 | Data bit 21 | DDR2_DIMM_DQ21 | SSTL-18 class I | AP13 |
| J19 pin 149 | Data bit 22 | DDR2_DIMM_DQ22 | SSTL-18 class I | AP14 |
| J19 pin 150 | Data bit 23 | DDR2_DIMM_DQ23 | SSTL-18 class I | AK15 |
| J19 pin 33 | Data bit 24 | DDR2_DIMM_DQ24 | SSTL-18 class I | AJ21 |
| J19 pin 34 | Data bit 25 | DDR2_DIMM_DQ25 | SSTL-18 class I | AM22 |
| J19 pin 39 | Data bit 26 | DDR2_DIMM_DQ26 | SSTL-18 class I | AN21 |
| J19 pin 40 | Data bit 27 | DDR2_DIMM_DQ27 | SSTL-18 class I | AP21 |
| J19 pin 152 | Data bit 28 | DDR2_DIMM_DQ28 | SSTL-18 class I | AJ20 |
| J19 pin 153 | Data bit 29 | DDR2_DIMM_DQ29 | SSTL-18 class I | AK21 |
| J19 pin 158 | Data bit 30 | DDR2_DIMM_DQ30 | SSTL-18 class I | AP20 |
| J19 pin 159 | Data bit 31 | DDR2_DIMM_DQ31 | SSTL-18 class I | AM21 |
| J19 pin 80 | Data bit 32 | DDR2_DIMM_DQ32 | SSTL-18 class I | AE20 |
| J19 pin 81 | Data bit 33 | DDR2_DIMM_DQ33 | SSTL-18 class I | AF21 |
| J19 pin 86 | Data bit 34 | DDR2_DIMM_DQ34 | SSTL-18 class I | AP24 |

**Table 2–45. DDR2 DIMM Interface I/O Signals (Part 3 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J19 pin 87 | Data bit 35 | DDR2_DIMM_DQ35 | SSTL-18 class I | AP26 |
| J19 pin 199 | Data bit 36 | DDR2_DIMM_DQ36 | SSTL-18 class I | AD21 |
| J19 pin 200 | Data bit 37 | DDR2_DIMM_DQ37 | SSTL-18 class I | AE21 |
| J19 pin 205 | Data bit 38 | DDR2_DIMM_DQ38 | SSTL-18 class I | AP23 |
| J19 pin 206 | Data bit 39 | DDR2_DIMM_DQ39 | SSTL-18 class I | AN24 |
| J19 pin 89 | Data bit 40 | DDR2_DIMM_DQ40 | SSTL-18 class I | AP27 |
| J19 pin 90 | Data bit 41 | DDR2_DIMM_DQ41 | SSTL-18 class I | AN27 |
| J19 pin 95 | Data bit 42 | DDR2_DIMM_DQ42 | SSTL-18 class I | AL28 |
| J19 pin 96 | Data bit 43 | DDR2_DIMM_DQ43 | SSTL-18 class I | AK25 |
| J19 pin 208 | Data bit 44 | DDR2_DIMM_DQ44 | SSTL-18 class I | AM26 |
| J19 pin 209 | Data bit 45 | DDR2_DIMM_DQ45 | SSTL-18 class I | AL26 |
| J19 pin 214 | Data bit 46 | DDR2_DIMM_DQ46 | SSTL-18 class I | AP29 |
| J19 pin 215 | Data bit 47 | DDR2_DIMM_DQ47 | SSTL-18 class I | AM28 |
| J19 pin 98 | Data bit 48 | DDR2_DIMM_DQ48 | SSTL-18 class I | AN30 |
| J19 pin 99 | Data bit 49 | DDR2_DIMM_DQ49 | SSTL-18 class I | AM30 |
| J19 pin 107 | Data bit 50 | DDR2_DIMM_DQ50 | SSTL-18 class I | AJ26 |
| J19 pin 108 | Data bit 51 | DDR2_DIMM_DQ51 | SSTL-18 class I | AH27 |
| J19 pin 217 | Data bit 52 | DDR2_DIMM_DQ52 | SSTL-18 class I | AM29 |
| J19 pin 218 | Data bit 53 | DDR2_DIMM_DQ53 | SSTL-18 class I | AL29 |
| J19 pin 226 | Data bit 54 | DDR2_DIMM_DQ54 | SSTL-18 class I | AJ29 |
| J19 pin 227 | Data bit 55 | DDR2_DIMM_DQ55 | SSTL-18 class I | AJ27 |
| J19 pin 110 | Data bit 56 | DDR2_DIMM_DQ56 | SSTL-18 class I | AF24 |
| J19 pin 111 | Data bit 57 | DDR2_DIMM_DQ57 | SSTL-18 class I | AG24 |
| J19 pin 116 | Data bit 58 | DDR2_DIMM_DQ58 | SSTL-18 class I | AF23 |
| J19 pin 117 | Data bit 59 | DDR2_DIMM_DQ59 | SSTL-18 class I | AN31 |
| J19 pin 229 | Data bit 60 | DDR2_DIMM_DQ60 | SSTL-18 class I | AH25 |
| J19 pin 230 | Data bit 61 | DDR2_DIMM_DQ61 | SSTL-18 class I | AH26 |
| J19 pin 235 | Data bit 62 | DDR2_DIMM_DQ62 | SSTL-18 class I | AP31 |
| J19 pin 236 | Data bit 63 | DDR2_DIMM_DQ63 | SSTL-18 class I | AP30 |
| J19 pin 42 | Data bit 64 | DDR2_DIMM_DQ64 | SSTL-18 class I | AH22 |
| J19 pin 43 | Data bit 65 | DDR2_DIMM_DQ65 | SSTL-18 class I | AM23 |
| J19 pin 48 | Data bit 66 | DDR2_DIMM_DQ66 | SSTL-18 class I | AJ23 |
| J19 pin 49 | Data bit 67 | DDR2_DIMM_DQ67 | SSTL-18 class I | AJ24 |
| J19 pin 161 | Data bit 68 | DDR2_DIMM_DQ68 | SSTL-18 class I | AK22 |
| J19 pin 162 | Data bit 69 | DDR2_DIMM_DQ69 | SSTL-18 class I | AL23 |
| J19 pin 167 | Data bit 70 | DDR2_DIMM_DQ70 | SSTL-18 class I | AL25 |
| J19 pin 168 | Data bit 71 | DDR2_DIMM_DQ71 | SSTL-18 class I | AK24 |
| J19 pin 6 | Data strobe bit 0 | DDR2_DIMM_DQS_N0 | SSTL-18 class I | AL11 |
| J19 pin 15 | Data strobe bit 1 | DDR2_DIMM_DQS_N1 | SSTL-18 class I | AN9 |

**Table 2–45. DDR2 DIMM Interface I/O Signals (Part 4 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| J19 pin 27 | Data strobe bit 2 | DDR2_DIMM_DQS_N2 | SSTL-18 class I | AJ14 |
| J19 pin 36 | Data strobe bit 3 | DDR2_DIMM_DQS_N3 | SSTL-18 class I | AP22 |
| J19 pin 83 | Data strobe bit 4 | DDR2_DIMM_DQS_N4 | SSTL-18 class I | AP25 |
| J19 pin 92 | Data strobe bit 5 | DDR2_DIMM_DQS_N5 | SSTL-18 class I | AP28 |
| J19 pin 104 | Data strobe bit 6 | DDR2_DIMM_DQS_N6 | SSTL-18 class I | AM32 |
| J19 pin 113 | Data strobe bit 7 | DDR2_DIMM_DQS_N7 | SSTL-18 class I | AP33 |
| J19 pin 45 | Data strobe bit 8 | DDR2_DIMM_DQS_N8 | SSTL-18 class I | AM24 |
| J19 pin 7 | Data strobe bit 0 | DDR2_DIMM_DQS_P0 | SSTL-18 class I | AL10 |
| J19 pin 16 | Data strobe bit 1 | DDR2_DIMM_DQS_P1 | SSTL-18 class I | AM9 |
| J19 pin 28 | Data strobe bit 2 | DDR2_DIMM_DQS_P2 | SSTL-18 class I | AH14 |
| J19 pin 37 | Data strobe bit 3 | DDR2_DIMM_DQS_P3 | SSTL-18 class I | AN22 |
| J19 pin 84 | Data strobe bit 4 | DDR2_DIMM_DQS_P4 | SSTL-18 class I | AN25 |
| J19 pin 93 | Data strobe bit 5 | DDR2_DIMM_DQS_P5 | SSTL-18 class I | AN28 |
| J19 pin 105 | Data strobe bit 6 | DDR2_DIMM_DQS_P6 | SSTL-18 class I | AM31 |
| J19 pin 114 | Data strobe bit 7 | DDR2_DIMM_DQS_P7 | SSTL-18 class I | AN33 |
| J19 pin 46 | Data strobe bit 8 | DDR2_DIMM_DQS_P8 | SSTL-18 class I | AL24 |
| J19 pin 195 | On-die termination control bit 0 | DDR2_DIMM_ODT0 | SSTL-18 class I | AE19 |
| J19 pin 77 | On-die termination control bit 1 | DDR2_DIMM_ODT1 | SSTL-18 class I | AD19 |
| J19 pin 52 | Clock enable bit 0 | DDR2_DIMM_CKE0 | SSTL-18 class I | AJ16 |
| J19 pin 171 | Clock enable bit 1 | DDR2_DIMM_CKE1 | SSTL-18 class I | AP7 |
| J19 pin 186 | Differential output clock 0 | DDR2_DIMM_CLK_N0 | SSTL-18 class I | AM14 |
| J19 pin 138 | Differential output clock 1 | DDR2_DIMM_CLK_N1 | SSTL-18 class I | AL13 |
| J19 pin 221 | Differential output clock 2 | DDR2_DIMM_CLK_N2 | SSTL-18 class I | AM15 |
| J19 pin 185 | Differential output clock 0 | DDR2_DIMM_CLK_P0 | SSTL-18 class I | AL14 |
| J19 pin 137 | Differential output clock 1 | DDR2_DIMM_CLK_P1 | SSTL-18 class I | AK13 |
| J19 pin 220 | Differential output clock 2 | DDR2_DIMM_CLK_P2 | SSTL-18 class I | AL15 |
| J19 pin 193 | Chip select | DDR2_DIMM_CSn0 | SSTL-18 class I | AG21 |
| J19 pin 76 | Chip select | DDR2_DIMM_CSn1 | SSTL-18 class I | AC22 |
| J19 pin 74 | Column address strobe | DDR2_DIMM_CASn | SSTL-18 class I | AD18 |
| J19 pin 192 | Row address strobe | DDR2_DIMM_RASn | SSTL-18 class I | AN19 |
| J19 pin 18 | Reset | DDR2_DIMM_RESETn | SSTL-18 class I | AE18 |
| J19 pin 120 | Presence-detect clock | DDR2_DIMM_SCL | SSTL-18 class I | AN15 |
| J19 pin 119 | Presence-detect data | DDR2_DIMM_SDA | SSTL-18 class I | AK19 |
| J19 pin 73 | Write enable | DDR2_DIMM_WEn | SSTL-18 class I | AJ19 |

Table 2–46 lists the DDR2 SDRAM DIMM component reference and manufacturing information.

**Table 2–46. DDR2 SDRAM DIMM Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| J19 | 400 MHz DIMM for 128 M × 72 (1 GByte plus ECC) | Micron Technology, Inc. | MT9HTF12872AY-800 | www.micron.com |

## DDR2 SDRAM Devices

The board supports two independent 8-bit DDR2 SDRAM interfaces on the horizontal I/O banks.

The target speed on the side bank is 300-MHz DDR.

Table 2–47 lists the DDR2 device A interface signals. JEDEC bus widths are used. Table 2–47 also shows a summary of the required number of pins to support the largest possible DDR2 devices available in a ×8 data configuration.

**Table 2–47. DDR2 Device A Interface I/O (Part 1 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| U17 pin H8 | Address bit 0 | DDR2_DEVA_A0 | SSTL-18 class I | U22-F34 |
| U17 pin H3 | Address bit 1 | DDR2_DEVA_A1 | SSTL-18 class I | U22-G34 |
| U17 pin H7 | Address bit 2 | DDR2_DEVA_A2 | SSTL-18 class I | U22-G31 |
| U17 pin J2 | Address bit 3 | DDR2_DEVA_A3 | SSTL-18 class I | U22-N24 |
| U17 pin J8 | Address bit 4 | DDR2_DEVA_A4 | SSTL-18 class I | U22-L29 |
| U17 pin J3 | Address bit 5 | DDR2_DEVA_A5 | SSTL-18 class I | U22-M30 |
| U17 pin J7 | Address bit 6 | DDR2_DEVA_A6 | SSTL-18 class I | U22-L31 |
| U17 pin K2 | Address bit 7 | DDR2_DEVA_A7 | SSTL-18 class I | U22-P25 |
| U17 pin K8 | Address bit 8 | DDR2_DEVA_A8 | SSTL-18 class I | U22-K33 |
| U17 pin K3 | Address bit 9 | DDR2_DEVA_A9 | SSTL-18 class I | U22-M29 |
| U17 pin H2 | Address bit 10 | DDR2_DEVA_A10 | SSTL-18 class I | U22-J34 |
| U17 pin K7 | Address bit 11 | DDR2_DEVA_A11 | SSTL-18 class I | U22-L32 |
| U17 pin L2 | Address bit 12 | DDR2_DEVA_A12 | SSTL-18 class I | U22-P23 |
| U17 pin L8 | Address bit 13 | DDR2_DEVA_A13 | SSTL-18 class I | U22-M26 |
| U17 pin L3 | Address bit 14 | DDR2_DEVA_A14 | SSTL-18 class I | U22-N26 |
| U17 pin G2 | Bank address bit 0 | DDR2_DEVA_BA0 | SSTL-18 class I | U22-H34 |
| U17 pin G3 | Bank address bit 1 | DDR2_DEVA_BA1 | SSTL-18 class I | U22-K30 |
| U17 pin G1 | Bank address bit 2 | DDR2_DEVA_BA2 | SSTL-18 class I | U22-J33 |
| U17 pin C8 | Data bit 0 | DDR2_DEVA_DQ0 | SSTL-18 class I | U22-K27 |
| U17 pin C2 | Data bit 1 | DDR2_DEVA_DQ1 | SSTL-18 class I | U22-J30 |
| U17 pin D7 | Data bit 2 | DDR2_DEVA_DQ2 | SSTL-18 class I | U22-K28 |
| U17 pin D3 | Data bit 3 | DDR2_DEVA_DQ3 | SSTL-18 class I | U22-J29 |
| U17 pin D1 | Data bit 4 | DDR2_DEVA_DQ4 | SSTL-18 class I | U22-H32 |

**Table 2–47. DDR2 Device A Interface I/O (Part 2 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| U17 pin D9 | Data bit 5 | DDR2_DEVA_DQ5 | SSTL-18 class I | U22-M24 |
| U17 pin B1 | Data bit 6 | DDR2_DEVA_DQ6 | SSTL-18 class I | U22-H31 |
| U17 pin B9 | Data bit 7 | DDR2_DEVA_DQ7 | SSTL-18 class I | U22-N25 |
| U17 pin A8 | Data strobe | DDR2_DEVA_DQS_N | SSTL-18 class I | U22-C34 |
| U17 pin B7 | Data strobe | DDR2_DEVA_DQS_P | SSTL-18 class I | U22-C33 |
| U17 pin F8 | Differential output clock | DDR2_DEVA_CK_N | SSTL-18 class I | U22-K32 |
| U17 pin E8 | Differential output clock | DDR2_DEVA_CK_P | SSTL-18 class I | U22-K31 |
| U17 pin F2 | Clock enable | DDR2_DEVA_CKE | SSTL-18 class I | U22-M27 |
| U17 pin G8 | Chip select | DDR2_DEVA_CSn | SSTL-18 class I | U22-E34 |
| U17 pin F3 | Write enable | DDR2_DEVA_WEn | SSTL-18 class I | U22-G33 |
| U17 pin G7 | Column address strobe | DDR2_DEVA_CASn | SSTL-18 class I | U22-G30 |
| U17 pin F7 | Row address strobe | DDR2_DEVA_RASn | SSTL-18 class I | U22-F32 |
| U17 pin B3 | Data write mask | DDR2_DEVA_DM | SSTL-18 class I | U22-F31 |
| U17 pin F9 | On-die termination control pin | DDR2_DEVA_ODT | SSTL-18 class I | U22-M28 |

Table 2–48 lists the DDR2 SDRAM devices A and B component reference and manufacturing information.

**Table 2–48. DDR2 SDRAM Devices A and B Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U17, U20 | 333 MHz devices for 32M ×8 (256 MBytes) | Micron Technology, Inc. | MT47H32M8BP-3:B | www.micron.com |

Table 2–49 lists the DDR2 device B interface signals. JEDEC bus widths are used.

**Table 2–49. DDR2 Device B Interface I/O (Part 1 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| U20 pin H8 | Address bit 0 | DDR2_DEVB_A0 | SSTL-18 class I | U22-R27 |
| U20 pin H3 | Address bit 1 | DDR2_DEVB_A1 | SSTL-18 class I | U22-R29 |
| U20 pin H7 | Address bit 2 | DDR2_DEVB_A2 | SSTL-18 class I | U22-J31 |
| U20 pin J2 | Address bit 3 | DDR2_DEVB_A3 | SSTL-18 class I | U22-U32 |
| U20 pin J8 | Address bit 4 | DDR2_DEVB_A4 | SSTL-18 class I | U22-K34 |
| U20 pin J3 | Address bit 5 | DDR2_DEVB_A5 | SSTL-18 class I | U22-T23 |
| U20 pin J7 | Address bit 6 | DDR2_DEVB_A6 | SSTL-18 class I | U22-M34 |
| U20 pin K2 | Address bit 7 | DDR2_DEVB_A7 | SSTL-18 class I | U22-U31 |
| U20 pin K8 | Address bit 8 | DDR2_DEVB_A8 | SSTL-18 class I | U22-R24 |
| U20 pin K3 | Address bit 9 | DDR2_DEVB_A9 | SSTL-18 class I | U22-V31 |
| U20 pin H2 | Address bit 10 | DDR2_DEVB_A10 | SSTL-18 class I | U22-P34 |
| U20 pin K7 | Address bit 11 | DDR2_DEVB_A11 | SSTL-18 class I | U22-T29 |

**Table 2–49. DDR2 Device B Interface I/O (Part 2 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| U20 pin L2 | Address bit 12 | DDR2_DEVB_A12 | SSTL-18 class I | U22-V32 |
| U20 pin L8 | Address bit 13 | DDR2_DEVB_A13 | SSTL-18 class I | U22-R28 |
| U20 pin L3 | Address bit 14 | DDR2_DEVB_A14 | SSTL-18 class I | U22-T30 |
| U20 pin G2 | Bank address bit 0 | DDR2_DEVB_BA0 | SSTL-18 class I | U22-N32 |
| U20 pin G3 | Bank address bit 1 | DDR2_DEVB_BA1 | SSTL-18 class I | U22-N33 |
| U20 pin G1 | Bank address bit 2 | DDR2_DEVB_BA2 | SSTL-18 class I | U22-R30 |
| U20 pin C8 | Data bit 0 | DDR2_DEVB_DQ0 | SSTL-18 class I | U22-P29 |
| U20 pin C2 | Data bit 1 | DDR2_DEVB_DQ1 | SSTL-18 class I | U22-P32 |
| U20 pin D7 | Data bit 2 | DDR2_DEVB_DQ2 | SSTL-18 class I | U22-N30 |
| U20 pin D3 | Data bit 3 | DDR2_DEVB_DQ3 | SSTL-18 class I | U22-N31 |
| U20 pin D1 | Data bit 4 | DDR2_DEVB_DQ4 | SSTL-18 class I | U22-R26 |
| U20 pin D9 | Data bit 5 | DDR2_DEVB_DQ5 | SSTL-18 class I | U22-P28 |
| U20 pin B1 | Data bit 6 | DDR2_DEVB_DQ6 | SSTL-18 class I | U22-R25 |
| U20 pin B9 | Data bit 7 | DDR2_DEVB_DQ7 | SSTL-18 class I | U22-N29 |
| U20 pin A8 | Data strobe | DDR2_DEVB_DQS_N | SSTL-18 class I | U22-L34 |
| U20 pin B7 | Data strobe | DDR2_DEVB_DQS_P | SSTL-18 class I | U22-M33 |
| U20 pin F8 | Differential output clock | DDR2_DEVB_CK_N | SSTL-18 class I | U22-R32 |
| U20 pin E8 | Differential output clock | DDR2_DEVB_CK_P | SSTL-18 class I | U22-P31 |
| U20 pin F2 | Clock enable | DDR2_DEVB_CKE | SSTL-18 class I | U22-N34 |
| U20 pin G8 | Chip select | DDR2_DEVB_CSn | SSTL-18 class I | U22-J32 |
| U20 pin F3 | Write enable | DDR2_DEVB_WEn | SSTL-18 class I | U22-T26 |
| U20 pin G7 | Column address strobe | DDR2_DEVB_CASn | SSTL-18 class I | U22-U25 |
| U20 pin F7 | Row address strobe | DDR2_DEVB_RASn | SSTL-18 class I | U22-D33 |
| U20 pin B3 | Data write mask | DDR2_DEVB_DM | SSTL-18 class I | U22-M31 |
| U20 pin F9 | On-die termination control pin | DDR2_DEVB_ODT | SSTL-18 class I | U22-D34 |

## QDRII+ SRAM

The board uses a burst-of-4 QDRII memory device for high-speed, low-latency memory access. The interface provides addressing for a 72-Mbit device. The actual device used may be 18, 36, or 72 Mbits. Because the Stratix III device supports 18 DQ/DQS group, the board uses a ×18 QDRII or QDRII+ SRAM device. QDRII+ SRAM is needed to support a QDRII rate that is greater than 300 MHz.

QDRII has separate read and write data ports with DDR interfaces operating up to 300 MHz. QDRII+ has separate read and write data ports with DDR interfaces operating up to 350 MHz. Burst-of-2 devices have a DDR address bus allowing for different read and write addresses on every clock (two data words per clock). Burst-of-4 devices have higher data rates due to the longer sequential addressing.

For QDRII devices, the interface supports 10.8 Gbps of throughput at 300 MHz (600 Mbps × 18 pins). The QDRII bandwidth doubles to 21.6 Gbps when considering combined read and write bandwidth. For QDRII+ devices, the interface supports 12.6 Gbps of throughput at 350 MHz (700 Mbps × 18 pins). The QDRII+ bandwidth doubles to 25.2 Gbps when considering combined read and write bandwidth.

Table 2–50 lists the QDRII interface pins.

**Table 2–50. QDRII Interface Pins (Part 1 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| U15 pin A9 | Address bit 0 | QDRII_A0 | 1.5-V HSTL class I | C17 |
| U15 pin B4 | Address bit 1 | QDRII_A1 | 1.5-V HSTL class I | C14 |
| U15 pin B8 | Address bit 2 | QDRII_A2 | 1.5-V HSTL class I | C16 |
| U15 pin C5 | Address bit 3 | QDRII_A3 | 1.5-V HSTL class I | A14 |
| U15 pin C7 | Address bit 4 | QDRII_A4 | 1.5-V HSTL class I | A15 |
| U15 pin N5 | Address bit 5 | QDRII_A5 | 1.5-V HSTL class I | F14 |
| U15 pin N6 | Address bit 6 | QDRII_A6 | 1.5-V HSTL class I | F15 |
| U15 pin N7 | Address bit 7 | QDRII_A7 | 1.5-V HSTL class I | A13 |
| U15 pin P4 | Address bit 8 | QDRII_A8 | 1.5-V HSTL class I | J15 |
| U15 pin P5 | Address bit 9 | QDRII_A9 | 1.5-V HSTL class I | G16 |
| U15 pin P7 | Address bit 10 | QDRII_A10 | 1.5-V HSTL class I | E14 |
| U15 pin P8 | Address bit 11 | QDRII_A11 | 1.5-V HSTL class I | B14 |
| U15 pin R3 | Address bit 12 | QDRII_A12 | 1.5-V HSTL class I | J16 |
| U15 pin R4 | Address bit 13 | QDRII_A13 | 1.5-V HSTL class I | H16 |
| U15 pin R5 | Address bit 14 | QDRII_A14 | 1.5-V HSTL class I | F12 |
| U15 pin R7 | Address bit 15 | QDRII_A15 | 1.5-V HSTL class I | D14 |
| U15 pin R8 | Address bit 16 | QDRII_A16 | 1.5-V HSTL class I | A10 |
| U15 pin R9 | Address bit 17 | QDRII_A17 | 1.5-V HSTL class I | B13 |
| U15 pin A3 | Address bit 18 | QDRII_A18 | 1.5-V HSTL class I | C15 |
| U15 pin A10 | Address bit 19 | QDRII_A19 | 1.5-V HSTL class I | E17 |
| U15 pin P10 | Write data bit 0 | QDRII_D0 | 1.5-V HSTL class I | A9 |
| U15 pin N11 | Write data bit 1 | QDRII_D1 | 1.5-V HSTL class I | B10 |
| U15 pin M11 | Write data bit 2 | QDRII_D2 | 1.5-V HSTL class I | B11 |
| U15 pin K10 | Write data bit 3 | QDRII_D3 | 1.5-V HSTL class I | A11 |
| U15 pin J11 | Write data bit 4 | QDRII_D4 | 1.5-V HSTL class I | E11 |
| U15 pin G11 | Write data bit 5 | QDRII_D5 | 1.5-V HSTL class I | A12 |
| U15 pin E10 | Write data bit 6 | QDRII_D6 | 1.5-V HSTL class I | C12 |
| U15 pin D11 | Write data bit 7 | QDRII_D7 | 1.5-V HSTL class I | D12 |
| U15 pin C11 | Write data bit 8 | QDRII_D8 | 1.5-V HSTL class I | D13 |
| U15 pin B3 | Write data bit 9 | QDRII_D9 | 1.5-V HSTL class I | L14 |
| U15 pin C3 | Write data bit 10 | QDRII_D10 | 1.5-V HSTL class I | K15 |
| U15 pin D2 | Write data bit 11 | QDRII_D11 | 1.5-V HSTL class I | K13 |

**Table 2–50. QDRII Interface Pins (Part 2 of 2)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number |
|---|---|---|---|---|
| U15 pin F3 | Write data bit 12 | QDRII_D12 | 1.5-V HSTL class I | K14 |
| U15 pin G2 | Write data bit 13 | QDRII_D13 | 1.5-V HSTL class I | G13 |
| U15 pin J3 | Write data bit 14 | QDRII_D14 | 1.5-V HSTL class I | D10 |
| U15 pin L3 | Write data bit 15 | QDRII_D15 | 1.5-V HSTL class I | F11 |
| U15 pin M3 | Write data bit 16 | QDRII_D16 | 1.5-V HSTL class I | F13 |
| U15 pin N2 | Write data bit 17 | QDRII_D17 | 1.5-V HSTL class I | G12 |
| U15 pin P11 | Read data bit 0 | QDRII_Q0 | 1.5-V HSTL class I | A3 |
| U15 pin M10 | Read data bit 1 | QDRII_Q1 | 1.5-V HSTL class I | B4 |
| U15 pin L11 | Read data bit 2 | QDRII_Q2 | 1.5-V HSTL class I | A4 |
| U15 pin K11 | Read data bit 3 | QDRII_Q3 | 1.5-V HSTL class I | A5 |
| U15 pin J10 | Read data bit 4 | QDRII_Q4 | 1.5-V HSTL class I | C6 |
| U15 pin F11 | Read data bit 5 | QDRII_Q5 | 1.5-V HSTL class I | F8 |
| U15 pin E11 | Read data bit 6 | QDRII_Q6 | 1.5-V HSTL class I | G9 |
| U15 pin C10 | Read data bit 7 | QDRII_Q7 | 1.5-V HSTL class I | F9 |
| U15 pin B11 | Read data bit 8 | QDRII_Q8 | 1.5-V HSTL class I | G10 |
| U15 pin B2 | Read data bit 9 | QDRII_Q9 | 1.5-V HSTL class I | J12 |
| U15 pin D3 | Read data bit 10 | QDRII_Q10 | 1.5-V HSTL class I | J11 |
| U15 pin E3 | Read data bit 11 | QDRII_Q11 | 1.5-V HSTL class I | G8 |
| U15 pin F2 | Read data bit 12 | QDRII_Q12 | 1.5-V HSTL class I | G11 |
| U15 pin G3 | Read data bit 13 | QDRII_Q13 | 1.5-V HSTL class I | B2 |
| U15 pin K3 | Read data bit 14 | QDRII_Q14 | 1.5-V HSTL class I | B5 |
| U15 pin L2 | Read data bit 15 | QDRII_Q15 | 1.5-V HSTL class I | F6 |
| U15 pin N3 | Read data bit 16 | QDRII_Q16 | 1.5-V HSTL class I | C5 |
| U15 pin P3 | Read data bit 17 | QDRII_Q17 | 1.5-V HSTL class I | D6 |
| U15 pin B7 | Byte write select bit 0 | QDRII_BWSn0 | 1.5-V HSTL class I | C11 |
| U15 pin A5 | Byte write select bit 1 | QDRII_BWSn1 | 1.5-V HSTL class I | D11 |
| U15 pin A11 | Echo clock | QDRII_CQ_N | 1.5-V HSTL class I | C4 |
| U15 pin A1 | Echo clock | QDRII_CQ_P | 1.5-V HSTL class I | H11 |
| U15 pin A6 | Write clock | QDRII_K_N | 1.5-V HSTL class I | H14 |
| U15 pin B6 | Write clock | QDRII_K_P | 1.5-V HSTL class I | J14 |
| U15 pin R6 | On-die termination pin for future QDRII devices. | QDRII_ODT | 1.5-V HSTL class I | C3 |
| U15 pin P6 | Valid output indicator | QDRII_QVLD | 1.5-V HSTL class I | A2 |
| U15 pin A8 | Read port select | QDRII_RPSn | 1.5-V HSTL class I | D17 |
| U15 pin A4 | Write port select | QDRII_WPSn | 1.5-V HSTL class I | K16 |

Table 2–51 lists the QDRII device component reference and manufacturing information.

**Table 2–51. QDRII Device Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U15 | 400 MHz QDRII+ burst-of-4 device for 2M × 18 | Cypress Semiconductor | CY7C1263V18-400BZXCES | www.cypress.com |

## P-SRAM

The board features 8 MBytes of P-SRAM memory with a 32-bit data bus. The devices use 1.8-V CMOS signaling and are optimized for low cost and power.

The 32-bit interface comprises two ×16 devices. The Samsung part features a maximum frequency of 104 MHz (104 Mbps). The theoretical bandwidth of the entire interface is 416 Mbps.

The P-SRAM devices are part of a shared bus with connectivity to the MAX II CPLD as well as the flash memory, which is called the FSM bus. All three devices use 1.8-V CMOS signaling. Altera recommends using the 5-Ω OCT setting on the FPGA and the one-half drive setting on the SRAM.

Table 2–52 lists the P-SRAM interface signal name, description, and signal type.

**Table 2–52. P-SRAM Device Pin-Out (Part 1 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Device Pin Number | Other Connections |
|---|---|---|---|---|---|
| U4 and U10 pin A3 | Address bus shared with flash and P-SRAM bit 1 | FSM_A1 | 1.8 V | H23 | U5 pin T8 and U9 pin B1 |
| U4 and U10 pin A4 | Address bus shared with flash and P-SRAM bit 2 | FSM_A2 | 1.8 V | G23 | U5 pin T9 and U9 pin C1 |
| U4 and U10 pin A5 | Address bus shared with flash and P-SRAM bit 3 | FSM_A3 | 1.8 V | F23 | U5 pin R9 and U9 pin D1 |
| U4 and U10 pin B3 | Address bus shared with flash and P-SRAM bit 4 | FSM_A4 | 1.8 V | D27 | U5 pin P9 and U9 pin D2 |
| U4 and U10 pin B4 | Address bus shared with flash and P-SRAM bit 5 | FSM_A5 | 1.8 V | D28 | U5 pin T10 and U9 pin A2 |
| U4 and U10 pin C3 | Address bus shared with flash and P-SRAM bit 6 | FSM_A6 | 1.8 V | F25 | U5 pin P13 and U9 pin C2 |
| U4 and U10 pin C4 | Address bus shared with flash and P-SRAM bit 7 | FSM_A7 | 1.8 V | F26 | U5 pin R10 and U9 pin A3 |
| U4 and U10 pin D4 | Address bus shared with flash and P-SRAM bit 8 | FSM_A8 | 1.8 V | G24 | U5 pin M10 and U9 pin B3 |
| U4 and U10 pin H2 | Address bus shared with flash and P-SRAM bit 9 | FSM_A9 | 1.8 V | F24 | U5 pin M11 and U9 pin C3 |
| U4 and U10 pin H3 | Address bus shared with flash and P-SRAM bit 10 | FSM_A10 | 1.8 V | E26 | U5 pin N10 and U9 pin C4 |

**Table 2–52. P-SRAM Device Pin-Out (Part 2 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Device Pin Number | Other Connections |
|---|---|---|---|---|---|
| U4 and U10 pin H4 | Address bus shared with flash and P-SRAM bit 11 | FSM_A11 | 1.8 V | D26 | U5 pin R11 and U9 pin C4 |
| U4 and U10 pin H5 | Address bus shared with flash and P-SRAM bit 12 | FSM_A12 | 1.8 V | A30 | U5 pin P10 and U9 pin A12 |
| U4 and U10 pin G3 | Address bus shared with flash and P-SRAM bit 13 | FSM_A13 | 1.8 V | A33 | U5 pin T12 and U9 pin B5 |
| U4 and U10 pin G4 | Address bus shared with flash and P-SRAM bit 14 | FSM_A14 | 1.8 V | B31 | U5 pin M11 and U9 pin C5 |
| U4 and U10 pin F3 | Address bus shared with flash and P-SRAM bit 15 | FSM_A15 | 1.8 V | A31 | U5 pin R12 and U9 pin D7 |
| U4 and U10 pin F4 | Address bus shared with flash and P-SRAM bit 16 | FSM_A16 | 1.8 V | B32 | U5 pin N11 and U9 pin D8 |
| U4 and U10 pin E4 | Address bus shared with flash and P-SRAM bit 17 | FSM_A17 | 1.8 V | A32 | U5 pin T13 and U9 pin A7 |
| U4 and U10 pin D3 | Address bus shared with flash and P-SRAM bit 18 | FSM_A18 | 1.8 V | M23 | U5 pin P11 and U9 pin B7 |
| U4 and U10 pin H1 | Address bus shared with flash and P-SRAM bit 19 | FSM_A19 | 1.8 V | L23 | U5 pin R13 and U9 pin C7 |
| U4 and U10 pin G2 | Address bus shared with flash and P-SRAM bit 20 | FSM_A20 | 1.8 V | B29 | U5 pin M1 and U9 pin C8 |
| U4 and U10 pin H6 | Address bus shared with flash and P-SRAM bit 21 | FSM_A21 | 1.8 V | C29 | U5 pin R14 and U9 pin A8 |
| U4 pin B6 | Data bus shared with flash and P-SRAM bit 0 | FSM_D0 | 1.8 V | G27 | U5 pin P4 and U9 pin E4 |
| U4 pin C5 | Data bus shared with flash and P-SRAM bit 1 | FSM_D1 | 1.8 V | F28 | U5 pin R1 and U9 pin E5 |
| U4 pin C6 | Data bus shared with flash and P-SRAM bit 2 | FSM_D2 | 1.8 V | E28 | U5 pin P5 and U9 pin G5 |
| U4 pin D5 | Data bus shared with flash and P-SRAM bit 3 | FSM_D3 | 1.8 V | D30 | U5 pin T2 and U9 pin G6 |
| U4 pin E5 | Data bus shared with flash and P-SRAM bit 4 | FSM_D4 | 1.8 V | C30 | U5 pin N5 and U9 pin H7 |
| U4 pin F5 | Data bus shared with flash and P-SRAM bit 5 | FSM_D5 | 1.8 V | F29 | U5 pin R3 and U9 pin E1 |
| U4 pin F6 | Data bus shared with flash and P-SRAM bit 6 | FSM_D6 | 1.8 V | E29 | U5 pin P6 and U9 pin E3 |
| U4 pin G6 | Data bus shared with flash and P-SRAM bit 7 | FSM_D7 | 1.8 V | J24 | U5 pin R4 and U9 pin F3 |
| U4 pin B1 | Data bus shared with flash and P-SRAM bit 8 | FSM_D8 | 1.8 V | J25 | U5 pin N6 and U9 pin F4 |
| U4 pin C1 | Data bus shared with flash and P-SRAM bit 9 | FSM_D9 | 1.8 V | A24 | U5 pin T4 and U9 pin F5 |

**Table 2–52. P-SRAM Device Pin-Out (Part 3 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Device Pin Number | Other Connections |
|---|---|---|---|---|---|
| U4 pin C2 | Data bus shared with flash and P-SRAM bit 10 | FSM_D10 | 1.8 V | A26 | U5 pin M6 and U9 pin H5 |
| U4 pin D2 | Data bus shared with flash and P-SRAM bit 11 | FSM_D11 | 1.8 V | B25 | U5 pin R5 and U9 pin G7 |
| U4 pin E2 | Data bus shared with flash and P-SRAM bit 12 | FSM_D12 | 1.8 V | A25 | U5 pin P7 and U9 pin E7 |
| U4 pin F2 | Data bus shared with flash and P-SRAM bit 13 | FSM_D13 | 1.8 V | J20 | U5 pin T5 and U9 pin H5 |
| U4 pin F1 | Data bus shared with flash and P-SRAM bit 14 | FSM_D14 | 1.8 V | K20 | U5 pin N7 and U9 pin G7 |
| U4 pin G1 | Data bus shared with flash and P-SRAM bit 15 | FSM_D15 | 1.8 V | K21 | U5 pin R6 and U9 pin E7 |
| U10 pin B6 | Data bus shared with flash and P-SRAM bit 16 | FSM_D16 | 1.8 V | K22 | U5 pin M7 |
| U10 pin C5 | Data bus shared with flash and P-SRAM bit 17 | FSM_D17 | 1.8 V | C26 | U5 pin T6 |
| U10 pin C6 | Data bus shared with flash and P-SRAM bit 18 | FSM_D18 | 1.8 V | B26 | U5 pin P14 |
| U10 pin D5 | Data bus shared with flash and P-SRAM bit 19 | FSM_D19 | 1.8 V | J22 | U5 pin R7 |
| U10 pin E5 | Data bus shared with flash and P-SRAM bit 20 | FSM_D20 | 1.8 V | J21 | U5 pin P8 |
| U10 pin F5 | Data bus shared with flash and P-SRAM bit 21 | FSM_D21 | 1.8 V | C24 | U5 pin T7 |
| U10 pin F6 | Data bus shared with flash and P-SRAM bit 22 | FSM_D22 | 1.8 V | E25 | U5 pin N8 |
| U10 pin G6 | Data bus shared with flash and P-SRAM bit 23 | FSM_D23 | 1.8 V | D25 | U5 pin R8 |
| U10 pin B1 | Data bus shared with flash and P-SRAM bit 24 | FSM_D24 | 1.8 V | D24 | U5 pin F12 |
| U10 pin C1 | Data bus shared with flash and P-SRAM bit 25 | FSM_D25 | 1.8 V | A27 | U5 pin D16 |
| U10 pin C2 | Data bus shared with flash and P-SRAM bit 26 | FSM_D26 | 1.8 V | A29 | U5 pin F13 |
| U10 pin D2 | Data bus shared with flash and P-SRAM bit 27 | FSM_D27 | 1.8 V | C27 | U5 pin D15 |
| U10 pin E2 | Data bus shared with flash and P-SRAM bit 28 | FSM_D28 | 1.8 V | C28 | U5 pin F14 |
| U10 pin F2 | Data bus shared with flash and P-SRAM bit 29 | FSM_D29 | 1.8 V | E23 | U5 pin D14 |
| U10 pin F1 | Data bus shared with flash and P-SRAM bit 30 | FSM_D30 | 1.8 V | D23 | U5 pin E12 |

**Table 2–52. P-SRAM Device Pin-Out (Part 4 of 4)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Device Pin Number | Other Connections |
|---|---|---|---|---|---|
| U10 pin G1 | Data bus shared with flash and P-SRAM bit 31 | FSM_D31 | 1.8 V | B28 | U5 pin C15 |
| U10 and U4 pin J3 | Address valid | SRAM_ADVn | 1.8 V | D21 | — |
| U4 pin A1 | Byte write select bit 0 | SRAM_BEn0 | 1.8 V | D22 | — |
| U4 pin B2 | Byte write select bit 1 | SRAM_BEn1 | 1.8 V | E22 | — |
| U10 pin A1 | Byte write select bit 2 | SRAM_BEn2 | 1.8 V | E20 | — |
| U10 pin B2 | Byte write select bit 3 | SRAM_BEn3 | 1.8 V | H20 | — |
| U10 and U4 pin J2 | Clock | SRAM_CLK | 1.8 V | C21 | — |
| U10 and U4 pin B5 | Chip select | SRAM_CSn | 1.8 V | A21 | — |
| U10 and U4 pin A2 | Output enable | SRAM_OEn | 1.8 V | A22 | — |
| U10 and U4 pin A6 | Power save mode | SRAM_PSn | 1.8 V | AL18 | — |
| U4 pin J1 | Data wait | SRAM_WAIT0 | 1.8 V | G20 | — |
| U10 pin J1 | Data wait | SRAM_WAIT1 | 1.8 V | F20 | — |
| U10 and U4 pin G5 | Write enable | SRAM_WEn | 1.8 V | B22 | — |

Figure 2–17 illustrates the latency for both fixed and variable modes of operation. For asynchronous accesses, each of the two devices has its own WAIT pin wired to the Stratix III device.

For Samsung SRAM pin definitions, data sheet, and other related documentation, refer to the Samsung website at www. samsung.com.

**Figure 2–17. SRAM Latency Timing Illustration**

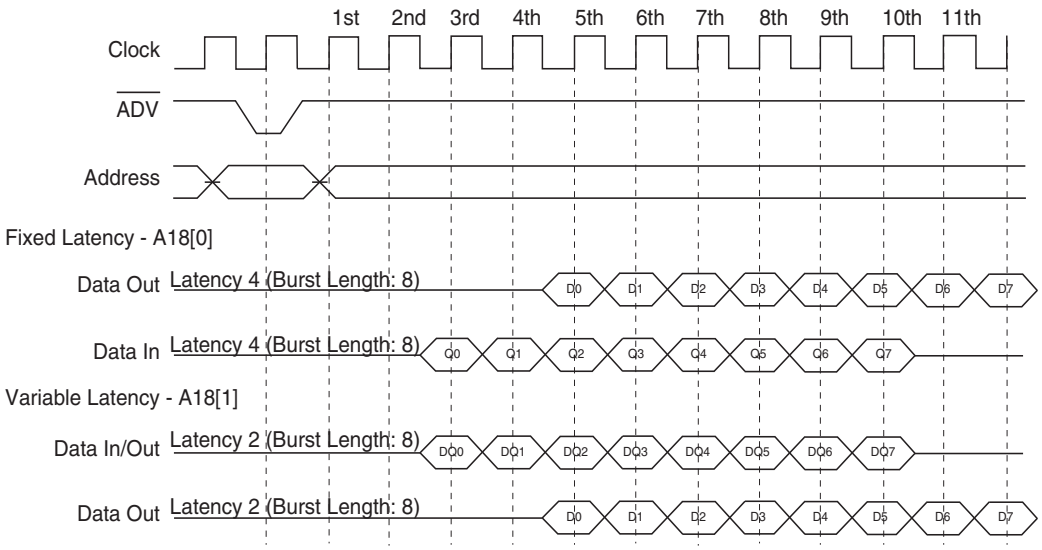


Table 2–53 lists the Samsung device latency values based on operation frequency.

**Table 2–53. SRAM Latency Vs. Frequency**

| Item | Up to 66 MHz | | Up to 80 MHz | | Up to 104 MHz | |
|---|---|---|---|---|---|---|
| | Fixed | Variable | Fixed | Variable | Fixed | Variable |
| Latency set (A11:A10:A9) | 4(0:0:1) | 2(1:0:0) | 5(0:1:0) | 3(0:0:0) | 7(1:0:1) | 4(0:0:1) |
| Read latency (min) | 4 | 2/4 | 5 | 3/5th | 7 | 4/7 |
| First read data fetch clock | 5th | 3rd/5th | 6th | 4th/6th | 8th | 5th/8th |
| Write latency (min) | 2 | 2 | 3 | 3 | 4 | 4 |
| First write data loading clock | 3rd | 3rd | 3rd | 4th | 5th | 5th |

Figure 2–18 and Figure 2–19 show the Samsung device read and write access waveforms.

**Figure 2–18. SRAM Read Timing Waveforms**

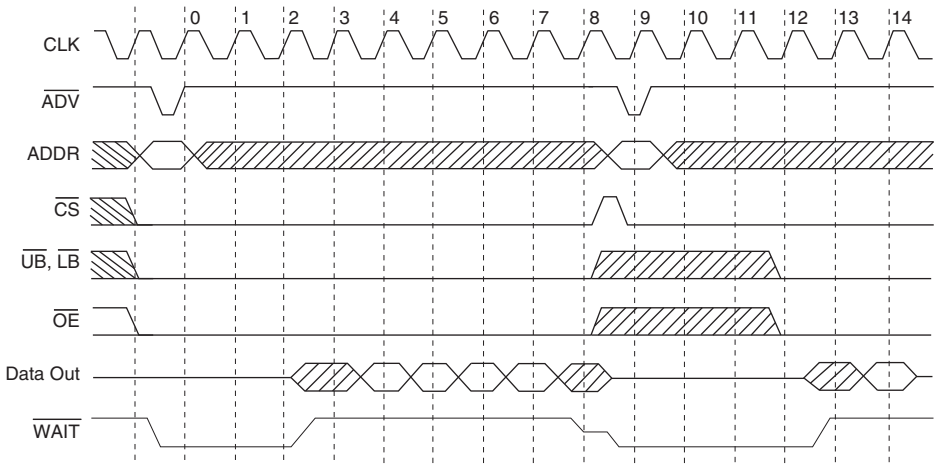



**Figure 2–19. SRAM Write Timing Waveforms**

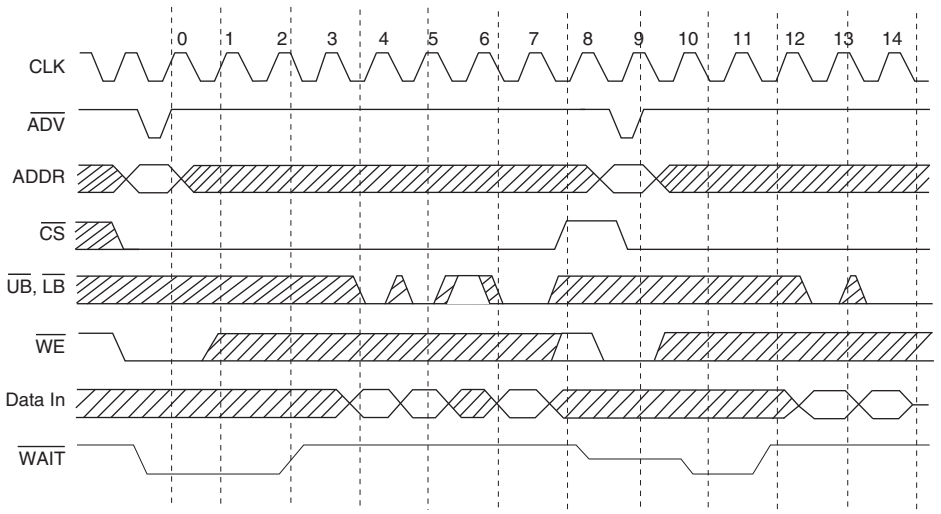


Table 2–54 lists the SRAM device component reference and manufacturing information.

**Table 2–54. SRAM Device Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U4, U10 | 32 MBytes (2M × 16) of SRAM | Samsung Semiconductor | K1B3216B2E-B170 | www.samsung.com |

## Flash Memory

A 512-Mbit Intel P30 flash memory device is used to store configuration files for the FPGA as well as any other necessary data for the development board operation. The target device is a PC48F4400P0VB00 in a BGA package and it supports the common flash interface (CFI) commands. The flash, SSRAM, and the MAX II CPLD all support 1.8-V I/O, and all three devices share a common address and data bus. The default addressing mode is a 16-bit word mode. Byte mode requires driving `BYTEn` low.

Table 2–55 lists the required flash memory signals.

**Table 2–55. Flash Interface I/O (Part 1 of 3)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| U9 pin B1 | Address bus shared with flash and P-SRAM bit 1 | FSM_A1 | 1.8 V | H23 | U5 pin T8 and U4 pin A3 and U10 pin A3 and U5 pin T8 |
| U9 pin C1 | Address bus shared with flash and P-SRAM bit 2 | FSM_A2 | 1.8 V | G23 | U5 pin T9 and U4 pin A4 and U10 pin A4 and U5 pin T9 |
| U9 pin D1 | Address bus shared with flash and P-SRAM bit 3 | FSM_A3 | 1.8 V | F23 | U5 pin R9 and U4 pin A5 and U10 pin A5 and U5 pin R9 |
| U9 pin D2 | Address bus shared with flash and P-SRAM bit 4 | FSM_A4 | 1.8 V | D27 | U5 pin P9 and U4 pin B3 and U10 pin B3 and U5 pin P9 |
| U9 pin A2 | Address bus shared with flash and P-SRAM bit 5 | FSM_A5 | 1.8 V | D28 | U5 pin T10 and U4 pin B4 and U10 pin B4 and U5 pin T10 |
| U9 pin C2 | Address bus shared with flash and P-SRAM bit 6 | FSM_A6 | 1.8 V | F25 | U5 pin P13 and U4 pin C3 and U10 pin C3 and U5 pin P13 |
| U9 pin A3 | Address bus shared with flash and P-SRAM bit 7 | FSM_A7 | 1.8 V | F26 | U5 pin R10 and U4 pin C4 and U10 pin C4 and U5 pin R10 |
| U9 pin B3 | Address bus shared with flash and P-SRAM bit 8 | FSM_A8 | 1.8 V | G24 | U5 pin M10 and U4 pin D4 and U10 pin D4 and U5 pin M10 |
| U9 pin C3 | Address bus shared with flash and P-SRAM bit 9 | FSM_A9 | 1.8 V | F24 | U5 pin M11 and U4 pin H2 and U10 pin H2 and U5 pin M11 |
| U9 pin D3 | Address bus shared with flash and P-SRAM bit 10 | FSM_A10 | 1.8 V | E26 | U5 pin N10 and U4 pin H3 and U10 pin H3 and U5 pin N10 |
| U9 pin C4 | Address bus shared with flash and P-SRAM bit 11 | FSM_A11 | 1.8 V | D26 | U5 pin R11 and U4 pin H4 and U10 pin H4 and U5 pin R11 |
| U9 pin A5 | Address bus shared with flash and P-SRAM bit 12 | FSM_A12 | 1.8 V | A30 | U5 pin P10 and U4 pin H5 and U10 pin H5 and U5 pin P10 |

**Table 2–55. Flash Interface I/O (Part 2 of 3)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| U9 pin B5 | Address bus shared with flash and P-SRAM bit 13 | FSM_A13 | 1.8 V | A33 | U5 pin T12 and U4 pin G3 and U10 pin G3 and U5 pin T12 |
| U9 pin C5 | Address bus shared with flash and P-SRAM bit 14 | FSM_A14 | 1.8 V | B31 | U5 pin M11 and U4 pin G4 and U10 pin G4 and U5 pin M11 |
| U9 pin D7 | Address bus shared with flash and P-SRAM bit 15 | FSM_A15 | 1.8 V | A31 | U5 pin R12 and U4 pin F3 and U10 pin F3 and U5 pin R12 |
| U9 pin D8 | Address bus shared with flash and P-SRAM bit 16 | FSM_A16 | 1.8 V | B32 | U5 pin N11 and U4 pin F4 and U10 pin F4 and U5 pin N11 |
| U9 pin A7 | Address bus shared with flash and P-SRAM bit 17 | FSM_A17 | 1.8 V | A32 | U5 pin T13 and U4 pin E4 and U10 pin E4 and U5 pin T13 |
| U9 pin B7 | Address bus shared with flash and P-SRAM bit 18 | FSM_A18 | 1.8 V | M23 | U5 pin P11 and U4 pin D3 and U10 pin D3 and U5 pin P11 |
| U9 pin C7 | Address bus shared with flash and P-SRAM bit 19 | FSM_A19 | 1.8 V | L23 | U5 pin R13 and U4 pin H1 and U10 pin H1 and U5 pin R13 |
| U9 pin C8 | Address bus shared with flash and P-SRAM bit 20 | FSM_A20 | 1.8 V | B29 | U5 pin M1 and U4 pin G2 and U10 pin G2 and U5 pin M1 |
| U9 pin A8 | Address bus shared with flash and P-SRAM bit 21 | FSM_A21 | 1.8 V | C29 | U5 pin R14 and U4 pin H6 and U10 pin H6 and U5 pin R14 |
| U9 pin G1 | Address bus shared with flash and P-SRAM bit 22 | FSM_A22 | 1.8 V | C31 | U5 pin N12 |
| U9 pin H8 | Address bus shared with flash and P-SRAM bit 23 | FSM_A23 | 1.8 V | D31 | U5 pin T15 |
| U9 pin B6 | Address bus shared with flash and P-SRAM bit 24 | FSM_A24 | 1.8 V | F27 | U5 pin P12 |
| U9 pin F2 | Data bus shared with flash and P-SRAM bit 0 | FSM_D0 | 1.8 V | G27 | U5 pin P4 and U4 pin B6 |
| U9 pin E2 | Data bus shared with flash and P-SRAM bit 1 | FSM_D1 | 1.8 V | F28 | U5 pin R1 and U4 pin C5 |
| U9 pin G3 | Data bus shared with flash and P-SRAM bit 2 | FSM_D2 | 1.8 V | E28 | U5 pin P5 and U4 pin C6 |
| U9 pin E4 | Data bus shared with flash and P-SRAM bit 3 | FSM_D3 | 1.8 V | D30 | U5 pin T2 and U4 pin D5 |
| U9 pin E5 | Data bus shared with flash and P-SRAM bit 4 | FSM_D4 | 1.8 V | C30 | U5 pin N5 and U4 pin E5 |
| U9 pin G5 | Data bus shared with flash and P-SRAM bit 5 | FSM_D5 | 1.8 V | F29 | U5 pin R3 and U4 pin F5 |
| U9 pin G6 | Data bus shared with flash and P-SRAM bit 6 | FSM_D6 | 1.8 V | E29 | U5 pin P6 and U4 pin F6 |
| U9 pin H7 | Data bus shared with flash and P-SRAM bit 7 | FSM_D7 | 1.8 V | J24 | U5 pin R4 and U4 pin G6 |
| U9 pin E1 | Data bus shared with flash and P-SRAM bit 8 | FSM_D8 | 1.8 V | J25 | U5 pin N6 and U4 pin B1 |
| U9 pin E3 | Data bus shared with flash and P-SRAM bit 9 | FSM_D9 | 1.8 V | A24 | U5 pin T4 and U4 pin C1 |

**Table 2–55. Flash Interface I/O (Part 3 of 3)**

| Board Reference | Description | Schematic Signal Name | I/O Standard | Stratix III Pin Number | Other Connections |
|---|---|---|---|---|---|
| U9 pin F3 | Data bus shared with flash and P-SRAM bit 10 | FSM_D10 | 1.8 V | A26 | U5 pin M6 and U4 pin C2 |
| U9 pin F4 | Data bus shared with flash and P-SRAM bit 11 | FSM_D11 | 1.8 V | B25 | U5 pin R5 and U4 pin D2 |
| U9 pin F5 | Data bus shared with flash and P-SRAM bit 12 | FSM_D12 | 1.8 V | A25 | U5 pin P7 and U4 pin E2 |
| U9 pin H5 | Data bus shared with flash and P-SRAM bit 13 | FSM_D13 | 1.8 V | J20 | U5 pin T5 and U4 pin F2 |
| U9 pin G7 | Data bus shared with flash and P-SRAM bit 14 | FSM_D14 | 1.8 V | K20 | U5 pin N7 and U4 pin F1 |
| U9 pin E7 | Data bus shared with flash and P-SRAM bit 15 | FSM_D15 | 1.8 V | K21 | U5 pin R6 and U4 pin G1 |
| U9 pin E6 | Clock | FLASH_CLK | 1.8 V | K24 | U5 pin L15 |
| U9 pin F6 | Address valid | FLASH_ADVn | 1.8 V | C7 | U5 pin L13 |
| U9 pin B4 | Chip enable | FLASH_CEn | 1.8 V | K25 | U5 pin K14 |
| U9 pin F8 | Output enable | FLASH_OEn | 1.8 V | K23 | U5 pin M16 |
| U9 pin F7 | Ready/busy | FLASH_RDYBSYn | 1.8 V | L16 | U5 pin L11 |
| U9 pin D4 | Reset | FLASH_RESETn | 1.8 V | E13 | U5 pin M15 |
| U9 pin G8 | Write enable | FLASH_WEn | 1.8 V | L22 | U5 pin L12 |

Table 2–56 shows the flash on-board memory map. The memory needs to provide non-volatile storage of a minimum of eight FPGA bit streams as well as various settings data used for on-board devices such as Ethernet TCP/IP defaults, PFL configuration bits, and data on the board itself. The remaining area is designated as user flash area for storage of software binaries and other data relevant to a user FPGA design.

**Table 2–56. Flash Memory Map (Part 1 of 2)**

| Name | Address |
|---|---|
| PFL option bits | 0x03FE.0000 |
| Ethernet option bits | 0x03FC.0000 |
| User space (10 MBytes) | 0x03FB.FFFF<br>0x0350.0000 |

**Table 2–56. Flash Memory Map (Part 2 of 2)**

| Name | Address |
|---|---|
| FPGA design 7 | 0x034E.FFFF<br>0x0000.0000 |
| FPGA design 6 | |
| FPGA design 5 | |
| FPGA design 4 | |
| FPGA design 3 | |
| FPGA design 2 | |
| FPGA design 1 | |
| FPGA design 0 (Default)<br>Factory design | |

Table 2–57 shows the flash sector map.

**Table 2–57. Flash Sector Map–Top and Bottom Parameter Dies**

| Die Stack Configuration | Size (KBytes) | 512-Mbit Flash (2 × 256 Mbits with 1 CE) | |
|---|---|---|---|
| | | Block | Address Range |
| 256-Mbit Top Parameter Die | 32 | 517 | 1FFC000–1FFFFFF |
| | ... | ... | ... |
| | 32 | 514 | 1FF0000–1FF3FFF |
| | 128 | 513 | 1FE0000–1FEFFFF |
| | ... | ... | ... |
| | 128 | 259 | 1000000–100FFFF |
| | | | |
| 256-Mbit Bottom Parameter Die | 128 | 258 | 770000–77FFFF |
| | ... | ... | 760000–76FFFF |
| | 128 | 4 | ... |
| | 32 | 3 | 010000– 01FFFF |
| | ... | ... | 000000–00FFFF |
| | 32 | 0 | ... |

For more read and write timing specification, refer to the Intel Corporation website at www.intel.com.

Table 2–58 lists the flash memory device component reference and manufacturing information.

**Table 2–58. Flash Memory Device Component Reference and Manufacturing Information**

| Board Reference | Description | Manufacturer | Manufacturing Part Number | Manufacturer Website |
|---|---|---|---|---|
| U9 | 512 Mbit, 1.7 to 2.0 V core, 64-pin BGA | Intel Corporation | PC48F4400P0VB00 | www.intel.com |

# Power Supply

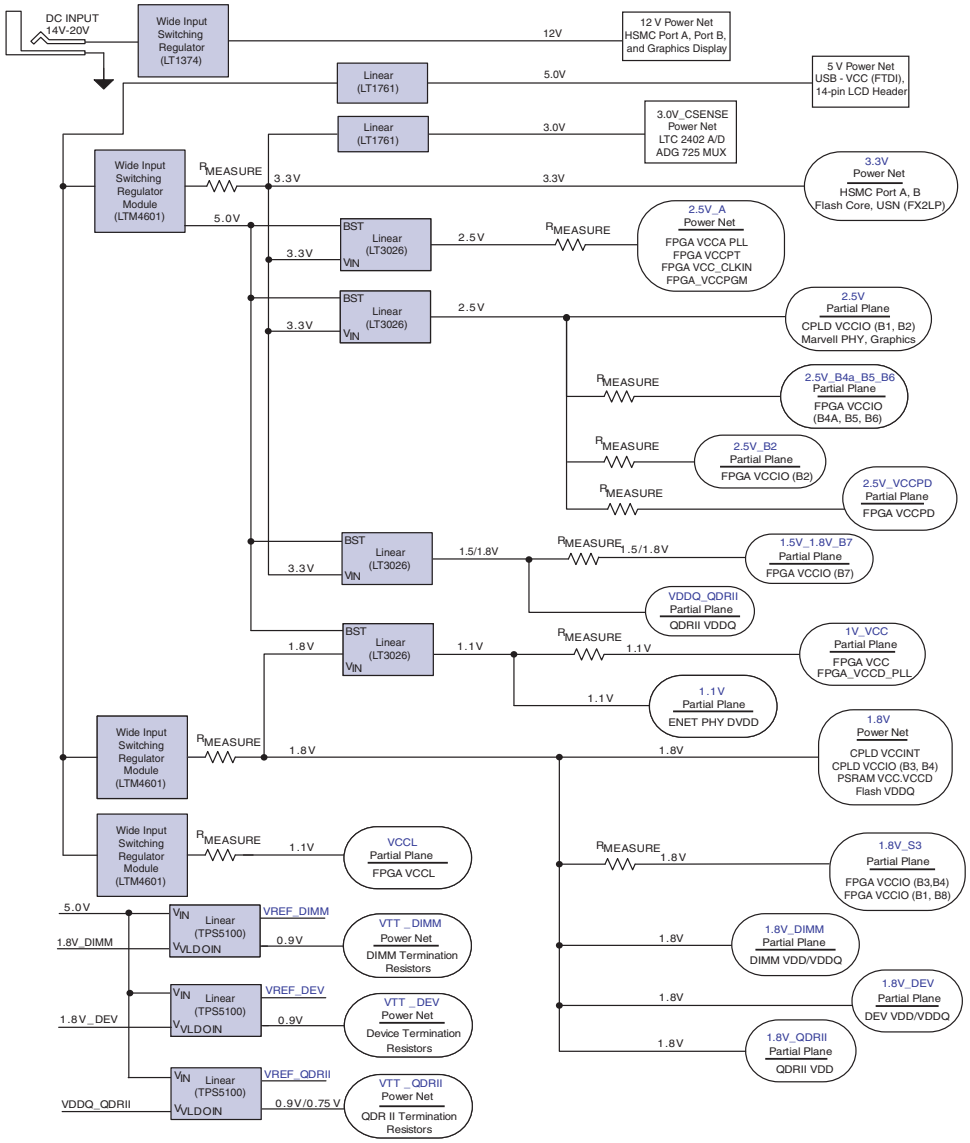
The board's power is provided through an IBM laptop style DC power input. The input voltage must be in the range of 14 V to 20 V. The DC voltage is then stepped down to the various power rails used by the components on the board and installed into the HSMC connectors.

An on-board, multi-channel A/D converter measures both voltage and current for several specific board rails. The power utilization is displayed on either the graphics display or the dedicated 7-segment display.

## Power Distribution System

Figure 2–20 shows the power distribution system, which uses current power rails. The currents shown reflect the regulator inefficiencies and regulator sharing.

**Figure 2–20. Power Distribution System**



## Power Measurement

Ten power supply rails have on-board voltage and current-sense capabilities. These devices and rails are split from the primary supply plane by a low-value sense resistor for the A/D converter to measure voltage and current.

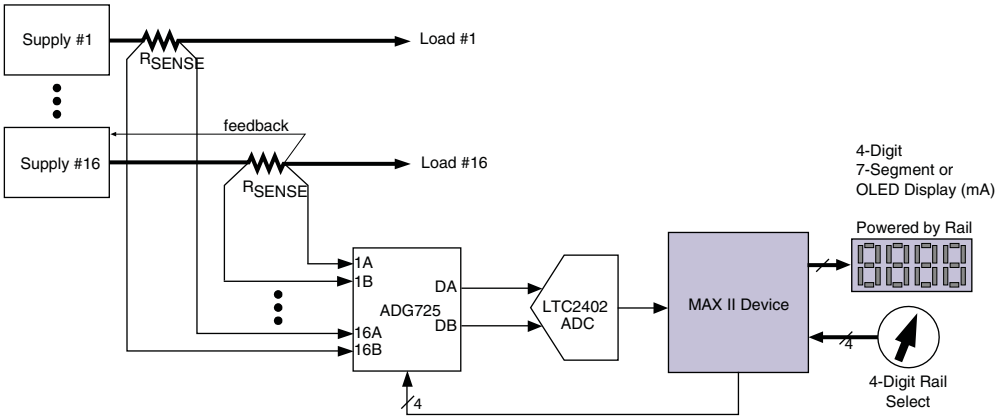
Table 2–59 shows the targeted rails where *Measured Net Name* column shows the name of the rail being measured, and the devices attached to that are listed under *Power Pin Name* and *Description* columns. If no subnet is named, then the power is the total output power for that voltage.

**Table 2–59. Power Measurement Rails**

| Number | Measured Net Name | Power Pin Name | Description |
|---|---|---|---|
| 1 | VCCL | VCCL | FPGA core power |
| 2 | 1.1V_VCC | VCC | FPGA I/O registers power |
| | | VCCD_PLL | FPGA PLL digital power |
| 3 | 2.5V_A | VCCPT | FPGA programmable power technology |
| | | VCCA_PLL | FPGA PLL analog power |
| 4 | 2.5V_VCCPD | VCCPD | Pre-driver power for I/Os |
| 5 | 2.5V_VCCPGM | VCCPGM | Power for configuration I/Os |
| 7 | 1.8V_S3 | VCCIO1A, VCCIO1C, VCCIO8A, VCCIO8B, VCCIO8C | FPGA I/O power banks 1, 8 |
| | | VCCIO3A, VCCIO3B, VCCIO3C, VCCIO4B, VCCIO4C | FPGA I/O power banks 3, 4 |
| 8 | 2.5V_B2 | VCCIO2A, VCCIO2C | FPGA I/O power bank 2 |
| 9 | 2.5V_B4A_B5_B6 | VCCIO4A, VCCIO5A, VCCIO5C, VCCIO6A, VCCIO6C | FPGA I/O power banks 4a, 5, 6 |
| 10 | 1.5V_1.8V_B7 | VCCIO7A, VCCIO7B, VCCIO7C | FPGA I/O power bank 7 |

This capability is realized using a 32-channel analog multiplexer to a 2-channel differential A/D converter, with a digital data bus connected to the MAX II CPLD. The CPLD contains a logic design that continually monitors the rails and displays the current in mA on the dedicated four-digit, 7-segment display or graphics display. Because only a single rail can be displayed at any time on the 7-segment display, an octal rotary switch is used to select which rail is currently being displayed. The sense resistor is large enough that it can be easily probed to confirm the display results. To see all of the currents at the same time, you can use the graphics display. Figure 2–21 illustrates the circuit.

**Figure 2–21. Power Measurement System**




## Security Key and Battery Backup

Stratix III devices are protected against copying, reverse engineering, and tampering using configuration bit-stream encryption. Specifically, the Stratix III devices use an advanced encryption standard (AES) algorithm with a 256-bit user-generated key. The key is stored on the Stratix III device and is used to decrypt the incoming configuration data bit-stream before configuration and initialization can begin.

This section discusses the following two methods of storing Stratix III device's 256-bit encryption key:

- Volatile
- Non-volatile

In the volatile scheme, the 256-bit key itself can be reprogrammed as needed. In this case, a 2.5-V battery is required to power the $V_{CCBAT}$ input and maintain the key within the Stratix III device when the system is powered off.

In the non-volatile scheme, the 256-bit key is programmed once into the Stratix III device and cannot be changed. The advantage of the non-volatile scheme is that a battery is not required to power the $V_{CCBAT}$ input.

By providing a 2.5-V coin battery connected to the $V_{CCBAT}$ power input, the board provides support for both volatile and non-volatile keys. A battery socket is also provided to allow battery replacement as needed. Additionally, the $V_{CCBAT}$ power input has a jumper to allow the VCCBAT pin to be tied directly to GND when the battery is removed for supporting the non-volatile key mode.

# Statement of China-RoHS Compliance

Table 2–60 lists hazardous substances included with the kit.

**Table 2–60. Table of Hazardous Substances' Name and Concentration** ***Notes*** (1), (2)

| Part Name | Lead (Pb) | Cadmium (Cd) | Hexavalent Chromium (Cr6+) | Mercury (Hg) | Polybrominated biphenyls (PBB) | Polybrominated diphenyl Ethers (PBDE) |
|---|---|---|---|---|---|---|
| Stratix III development board | X* | 0 | 0 | 0 | 0 | 0 |
| 12 V power supply | 0 | 0 | 0 | 0 | 0 | 0 |
| Type A-B USB cable | 0 | 0 | 0 | 0 | 0 | 0 |
| User guide | 0 | 0 | 0 | 0 | 0 | 0 |

**Notes to Table 2–60:**

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

This chapter provides additional information about the document and Altera.

## Document Revision History

The following table lists the revision history for this document.

| Date | Version | Changes |
|---|---|---|
| May 2013 | 1.5 | ■ Updated the MAX II pin assignment for FSM_A9 signal in Table 2–5.<br>■ Updated the Stratix III pin numbers for DDR2_DEVA_A12,DDR2_DEVA_A13,DDR2_DEVA_A14,DDR2_DEVA_BA0,DDR2_DEVA_BA1,DDR2_DEVA_BA2,and DDR2_DEVA_CASn signals in Table 2–47.<br>■ Updated the Stratix III pin numbers for DDR2_DEVB_DQ2 and DDR2_DEVB_DQ3 signals in Table 2–49.<br>■ Updated the document template. |
| November 2008 | 1.4 | ■ Updated QDRII interface pin information in Table 2–50. |
| November 2008 | 1.3 | ■ Updated DDR2 DIMM board memory size.<br>■ Updated Stratix III pin numbers for the differential output clock signals in Table 2–45. |
| August 2008 | 1.2 | ■ Updated JTAGS settings in Table 2–7.<br>■ Updated "Power Select Rotary Switch" section.<br>■ Corrected pin description in Table 2–32.<br>■ Updated pin description in Table 2–39.<br>■ Updated "High-Speed Mezzanine Cards" section.<br>■ Corrected pin description in Table 2–41 and Table 2–42.<br>■ Corrected pin numbers in Table 2–47 and Table 2–49. |
| March 2008 | 1.1 | Corrected minor errors and incorporated device errata. |
| December 2007 | 1.0 | First publication |

# How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

| Contact (1) | Contact Method | Address |
|---|---|---|
| Technical support | Website | www.altera.com/support |
| Technical training | Website | www.altera.com/training |
| | Email | custrain@altera.com |
| Product literature | Website | www.altera.com/literature |
| Nontechnical support (general) | Email | nacomp@altera.com |
| (software licensing) | Email | authorization@altera.com |

**Note to Table:**

(1) You can also contact your local Altera sales office or sales representative.

# Typographic Conventions

The following table shows the typographic conventions this document uses.

| Visual Cue | Meaning |
|---|---|
| **Bold Type with Initial Capital Letters** | Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI. |
| **bold type** | Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file. |
| *Italic Type with Initial Capital Letters* | Indicate document titles. For example, *Stratix IV Design Guidelines*. |
| *italic type* | Indicates variables. For example, *n* + 1.<br>Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>*.**pof** file. |
| Initial Capital Letters | Indicate keyboard keys and menu names. For example, the Delete key and the Options menu. |
| "Subheading Title" | Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions." |
| `Courier type` | Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`.<br>Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`.<br>Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`). |
| ↵ | An angled arrow instructs you to press the Enter key. |
| 1., 2., 3., and<br>a., b., c., and so on | Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure. |
| ■ ■ ■ | Bullets indicate a list of items when the sequence of the items is not important. |
|  | The hand points to information that requires special attention. |

| Visual Cue | Meaning |
|---|---|
|  | The question mark directs you to a software help system with related information. |
|  | The feet direct you to another document or website with related information. |
|  | The multimedia icon directs you to a related multimedia presentation. |
|   | A caution calls attention to a condition or possible situation that can damage or destroy the product or your work. |
|   | A warning calls attention to a condition or possible situation that can cause you injury. |
|  | The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents. |
|  | The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document. |